64000

HP64000 Logic Development System

Model 64623A 20 Channel State Acquisition Board

HEWLETT PACKARD

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Service Manual, Model 64623A
20 Channel State Acquisition Board
64623-90902, September 1983

Your comments are important to us. Please answer this questionaire and return it to us. Circle the number that best describes your answer in questions 1 through 7. Thank you.

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HEWLETT PACKARD

SERVICE MANUAL

MODEL 64623A
20 CHANNEL STATE ACQUISITION BOARD

REPAIR NUMBERS

This manual applies to 64623A 20 Channel State Acquisition Boards with a repair number prefix of 2325A. For further information on repair numbers refer to "Instruments Covered by This Manual" in Section I, and Section VII for Backdating to earlier Models.

Manual Part No. 64623-90902
Microfiche Part No. 64623-90802

PRINTED: September 1983

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with the power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

Table of Contents

Section VI Replaceable parts

Section VII Manual Backdating

Section VIII Service

List of Figures and Tables

Figure or Table Page

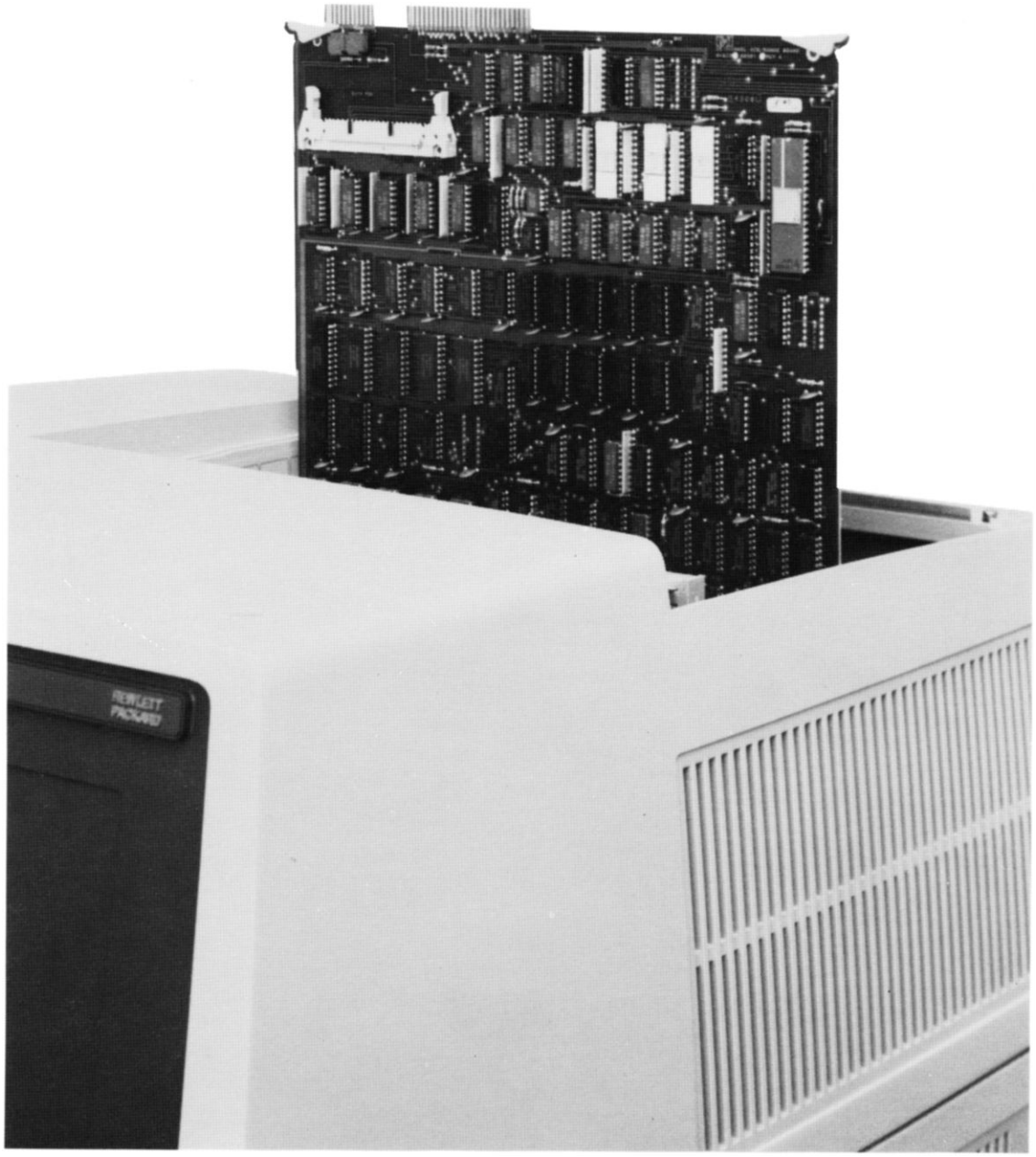


Figure 1-1. Model 64621A 20 Channel Acquisition Board

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This Service Manual contains information required to install, test and service the Hewlett-Packard Model 64623A 20 Channel State Acquisition Board (20 Ch ACQ). Operating instructions are provided in a separate Operating Manual supplied with the instrument. It should be kept with the instrument for use by the operator.

1-3. Shown on the title page is a microfiche part number. This number can be used to order 4x6-inch microfilm transparencies of the manual. Each microfiche contains up to 96 photoduplicates of the manual pages.

1-4. SPECIFICATIONS.

1-5. Normally instrument specifications are listed in this section. However, the Model 64623A 20 Channel State Acquisition Board cannot function without a Model 64621A State Analysis Control Board, and for the State Analysis Subsystem Specifications the two models are considered as one unit. Therefore, the specifications are listed only in the Model 64621A State Analysis Control Board Service Manual, Section I, General Information.

1-6. INSTRUMENTS COVERED BY THIS MANUAL.

1-7. Attached to the instrument or printed on the printed circuit board is the repair number. The repair number is in the form: 0000A0000. It is in two parts; the first four digits and the letter are the repair prefix, and the last five are the suffix. The prefix is the same for all identical instruments. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the repair number prefix(es) listed under REPAIR NUMBERS on the title page.

1-8. An instrument manufactured after the printing of this manual may have a repair number prefix that is not listed on the title page. This unlisted repair number prefix indicates that the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a Manual Changes supplement. This supplement contains "change information" that explains how to adapt the manual for the newer instrument.

1-9. In addition to change information, the supplement contains information for correcting errors in the manual. To keep this manual as current as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-10. For information concerning a repair number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard Office.

1-11. RECOMMENDED TEST EQUIPMENT.

1-12. Equipment required to maintain the Model 64623A is listed in Table 1-1. Other equipment may be substituted if it meets or exceeds the critical specifications listed in the table.

Table 1-1. Recommended Test Equipment

4 1/2 Digit Multimeter with +/ 1 mV accuracy.....HP Model 3466A

Signature Multimeter.....HP Model 5005A

Dual Channel 100 MHz Oscilloscope with probes.....HP Model 1743A

1-13. DESCRIPTION.

1-14. The State Analyzer is used to monitor information flow in the data domain. The information may be a software program, the actions of a hardware state machine, or random logic signals.

1-15. The State Analyzer consists of one Model 64621A State Analysis Control Board, and from one to three State Data Acquisition Boards. The State Data Acquisition Boards may be the 40 Channel State Data Acquisition Board, the 20 Channel State Data Acquisition Board, or a combination of the two Acquisition Boards. The State Analyzer will have the necessary number of Data and Clock Probes for the Acquisition Boards used (Models 64635A and 64636A).

1-16. Up to three Acquisition Boards may be combined to form a State Analyzer with as many as 120 channels.

1-17. Logic Analyzers within one Mainframe may be connected together using the Inter Module Bus (IMB). One possible use of the IMB is to allow a State Analyzer to trigger a Timing Analyzer.

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information for installing and removing the Model 64623A. Included are initial inspection procedures, preparation for use, and instructions for repacking the instrument for shipment.

2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. Procedures for checking electrical performance are given in Section IV. If the contents are not complete, if there is mechanical damage or defect, or if the instrument does not pass the Performance Tests, notify the nearest Hewlett-Packard Office. If the shipping container is damaged, or if the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard Office. Keep the shipping materials for carrier's inspection. The HP office will arrange for repair or replacement at HP option without waiting for claim settlement.

2-5. PREPARATION FOR USE.

2-6. There are no specific preparation for use procedures except the actual installation of the boards in the Mainframe cardcage.

2-7. INSTALLATION INSTRUCTIONS.

2-8. The 64623A 20 Channel State Acquisition Board will work only when used with a 64621A State Control Board. Therefore, the installation and removal procedure is not documented here. Refer to the 64621A State Control Service Manual for installation and removal instructions. (Includes Synchrounous Expansion Bus (SEB) and Inter Module Bus (IMB).)

2-9. STORAGE AND SHIPMENT.

2-10. ENVIRONMENT.

2-11. This instrument may be stored or shipped in environments within the following limits:

Temperature	-40 Deg C to +75 Deg C
Humidity	5% to 80%
Altitude	15000 M (50000 ft)

The instrument should also be protected from temperature extremes which cause condensation within the instrument.

2-12. PACKING.

2-13. Tagging for Service. If the instrument is to be shipped to a Hewlett-Packard Sales/Service Office for service or repair, attach a tag showing owner (with address), complete instrument repair number, and a description of the service required.

2-14. Original Packing. Containers and materials identical to those used in factory packing are available through Hewlett-Packard Offices. Mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and complete repair number.

2-15. Other Packing. The following general instructions should be used for repacking with commercially available materials:

a. Wrap instrument in heavy plastic or paper. (If shipping to Hewlett-Packard Office or Service Center, attach a tag indicating type of service required, return address, model number, and complete repair number.

b. Use a strong shipping container. A double wall carton made of 350 pound test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 inches) thick around all sides of the instrument to provide firm cushioning and prevent movement inside container.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to instrument by model number and complete repair number.

SECTION III

OPERATION

3-1. INTRODUCTION.

3-2. The operation of the Model 64623A is a function of the system software. Complete operation from the keyboard of the system is beyond the scope of the Service Manual. Please refer to the Operator's Manuals for the procedure.

NOTES

SECTION IV

PERFORMANCE VERIFICATION

4-1. INTRODUCTION.

4-2. This section describes the Performance Verification (opt_test) for Model 64623A 20 Channel State Acquisition Board. This section consists of three parts; 1. Operation Verification, 2. Performance Verification, and 3. Troubleshooting.

4-3. With the exception of the continuity test on the probes, the Operation Verification tests are all automatic and require no test equipment or dissassembly of the Mainframe. The Operation Verification provides a 90% assurance that the Model 64623A meets all specifications.

4-4. The Performance Verification tests require test equipment and disassembly of the Mainframe. The Performance Verification tests involve manual testing and verification of specifications. Therefore, the Performance Verification Tests should be run only by a qualified service person.

4-5. The Performance Verification tests are divided into two parts; 1. automated tests and 2. manual tests. The automated tests must pass before performing the manual tests.

NOTE

Before running the following tests, insure the boards are installed as indicated in Section II of the 64621A State Analysis Service Manual. Both Operation Tests and Performance Tests must be run to insure that the Model 64623A meets all specifications after repair.

4-6. The Troubleshooting portion of this section describes the tests, shows the displays for the tests, decodes the displays, and tells how to use the tests with Signature Analysis for troubleshooting.

4-7. OPERATION VERIFICATION.

a. Press opt-test. RETURN.

b. Press SLOT # (of 20 Channel Acquisition Board) RETURN.

c. Press run all_boards. RETURN.

d. The status line near the bottom should read "STATUS: 10 MHz Verification PASSED".

e. Run the continuity tests as outlined in Section IV of the Model 64635A General Purpose Data Probe, and the Model 64636A General Purpose Clock Probe Service Manuals.

4-8. The State Control board (Control board) must pass Operation Verification before a State Acquisition board (Acquisition board) will pass.

4-9. If a failure occurred, refer to the paragraph on Troubleshooting in Section IV of the appropriate manual. This manual covers only the automatic tests for the 20 Channel Acquisition Board and signature analysis for the Data Probe interface on the 20 Channnel Acquisition Board.

4-10. PERFORMANCE VERIFICATION.

4-11. First run the Automated Tests (repeat the Operation Verification), then perform the Manual Tests.

4-12. AUTOMATED TESTS.

a. Press opt-test. RETURN.

b. Press SLOT # of 20 Channel Acquisition Board. RETURN.

c. Press run all_boards. RETURN.

d. The status line near the bottom should read "STATUS: 10 MHz Verification PASSED".

e. Run the continuity tests as outlined in Section IV of the Model 64635A General Purpose Data Probe, and the Model 64636A General Purpose Clock Probe Service Manuals.

4-13. MANUAL TESTS.

4-14. Refer to the Model 64621A State Analysis Control Board Service Manual, Section IV, Manual Tests for the procedures to test Pulse Widths, and Setup and Hold Times.

4-15. TROUBLESHOOTING.

4-16. General Comments. First, determine if the 20 Channel Acq Board tests failed by pressing: display, SLOT # (of 20 Channel Acq Board), RETURN. Troubleshoot the first test that failed, then re-run Operation Verification. The automatic tests listed in Figure 4-1 are interdependent so that all tests preceeding a given test must pass for the given test to pass.

4-17. If the failure was a data probe and the 20 Channel Acq Board is suspected, go to the test description for the "Data Probe Interface test" which follows Test 9.

4-18. Test 10 is used in Section V, Adjustments.

4-19. Each automatic test is now described, and a signature analysis path provided. Each SA path works its way from the test output back towards the inputs. To run a particular test, press opt_test then RETURN. Press SLOT # (of the 20 Channel Acq Board) then RETURN. Finally, press run, SLOT # , test, test # (of first failing test) , repeat, then RETURN. This causes the test to repeat and allows signatures to be taken. Examples of valid commands while operating the State Analysis Performance Verification are as follows:

a. run 5 test 8 RETURN . This command will cause test 5 to be performed once on the board in slot 8.

b. display 2 RETURN . This command will cause the test results of all tests on the board in slot 2 to be displayed. It will not run any test.

4-20. Various other commands are prompted by the softkeys, e.g., "repeat" makes a test cycle; "stop" halts the test in progress after it has completed a cycle; "list file_name" writes the display to a designated file; "end" returns the user to option_test PV by stopping the State Analysis PV.

4-21. When a bit pattern is given (e.g. data 00000100), the 1 indicates that bit 2 has failed. In all cases, a 0 indicates pass and a 1 indicates failure; the msb is to the extreme left; all patterns start with bit 0 as the lsb unless otherwise noted.

4-22. The Synchronous Expansion Bus (SEB) connects the State Control board to State Acquisition boards. The SEB is tested here for the first time. Test failure could be due to faulty seating of the SEB Cable (50 pin ribbon cable across the top of the State Cards), or to a component failure on the State Control board. Signatures for the SEB interface on the Control Board have been provided for each test as applicable. If a spare Control Board is available, it is advisable to isolate the problem to the board level before using SA. It is necessary to use an extender wire on the 5005 pod to read the LMAP2 signal on the extender card when probing the Control Board.

10 MHz State Test: Board in Slot 3 Pass Tested: 1 Failed: 0

Test	Slot 3: 20 Channel Acquisition	Tested	Failed
Automatic Tests			
1	Interaction with control board and stimulus	1	0
2	Resource Patterns	1	0
3	Sequence Patterns	1	0
4	Trace memory	1	0
5	Overview event memory	1	0
6	Overview/Range decode RAMs	1	0
7	Overview/Range functions	1	0
8	State count	1	0
9	Other counter tests	1	0
Manual Tests			
10	Threshold circuit calibration	0	

Figure 4-1. Automatic Tests

4-23. TEST 1. CONTROL BOARD and STIMULUS. LOOP A

4-24. Purpose -to verify that a strobe request generated by this board is received by the Control board, and to stimulate the Data Pod Threshold D/A Converter (DAC).

4-25. How -strobe request (PBSTBRQ) is sent to the Control board where it resets the Slow Clock Detector.

4-26. Results -since the Strobe Generator and Slow Clock Dectector were tested during the Control board operation verification, failure is due, most likely, to the absence of the SEB cable. "Release data bus" is a read of the mainframe data bus when nothing is addressed; failure indicates that a card in the cardcage is causing problems on the bus. The stimulus portion of this test is write-only, therefore, no results are given for it.

```
10 MHz Stat  Test: Board in Slot 3        Pass  Tested:  1   Failed:  0

  Slot  3: 20 Channel Acquisition
  Test  1: Interaction with control board and stimulus

  Strobe Request   Pass

  Release data bus 0000000000000000
```

Figure 4-2. Interaction With Control Board

4-27. Stimulus -A staircase ramp is produced by the DAC during this test. See Figure 4-3. The DAC is tested in the Data Probe Interface test, also, it is stimulated by test 10.

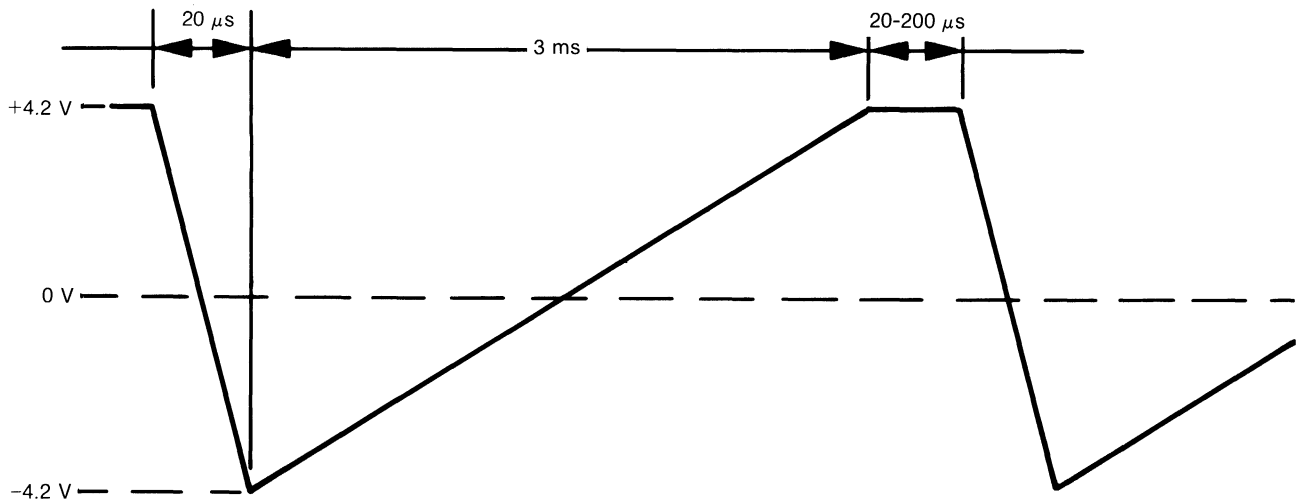


Figure 4-3. Stimulus

4-28. Loop A Signature Path for Strobe Request: U52 (CTL BD), U116, U101.

Loop A Singature Path for DAC: U34, U83, U115, U114.

4-29. TEST 2: RESOURCE PATTERNS. LOOP B

NOTE: Failures in Tests 5, 6, or 7 can cause a failure in this test. This is due to LBRP0-3 being wire ORed from U3 in the Resource Pattern Recognition Circuits and U4 in the Overview Event/Range Decode Circuits.

4-30. Purpose -to verify the Mainframe Interface, the State Recognition Latch/Counters, and the Resource Pattern Recognition circuitry.

4-31. How -The Resource Pattern Trigger Memories are loaded via the Mainframe Interface and using the State Recognition Latch/Counter in the count mode. The actual Resource Patterns are bussed to the Control Board (LBRP0-7) and interpreted by the Analysis Controller. SEB signals used during this test are LBRP0-7 and the state recognition strobe PBSRS and NBSRS.

4-32. Results -The Analysis Controller is programmed to decode the Resource Patterns (LBRP0-7) and output a trigger (NTRIG). Note that the Resource Patterns are wire ORed with the Event Range/Decode outputs; they may be the cause of the failure.

```
10 MHz State Test: Board in Slot 3        Pass  Tested:  1   Failed:  0

  Slot  3: 20 Channel Acquisition
  Test  2: Resource Patterns


 Resource Pattern:  76543210   (1 = Error)

 All patterns true  00000000
 All patterns false 00000000

 Data bits:  0 to  3 00000000  RAM Adrs:  Pass
             4 to  7 00000000              Pass
             8 to 11 00000000              Pass
            12 to 15 00000000              Pass
            16 to 19 00000000              Pass
```

Figure 4-4. Resource Patterns

4-33. Figure 4-4 Interpretation.

```
All patterns true   00000000
All patterns false  00000000
```

(Eight bit output of U14 and U3. All patterns true is all highs. All patterns false drives the outputs low.)

```
Data bits: 0 to  3  00000000   RAM Adrs:  Pass
           4 to  7  00000000              Pass
           8 to 11  00000000              Pass
          12 to 15  00000000              Pass
          16 to 19  00000000              Pass
```

(the data bits, 0 to 20, refer to SYND0 to SYND19; they are used as address lines A0-A3 on the Resource Pattern Trigger Memories. The eight bit pattern output by each pair of RAMs becomes LBRP0-7. The RAM Address on the display refers to the RAM select lines LWR0-4.)

4-34. Loop B Signature Path: U1 (CTL BD), U3, U14, Resource Pattern Trigger Memories U51 -U55 and U66 -U70, State Recognition Latch/Counters U83, U114, U115.

4-35. TEST 3: SEQUENCE PATTERNS. LOOPS C and D

4-36. Purpose - to verify Sequence Pattern Recognition Circuitry.

4-37. Control Board Circuitry involved -Sequence States output by U42(CTL BD) as BSS0-3; Sequence Patterns received by U17(CTL BD) as LBSP0-3. Strobe Generator tested in Test 2 (Control Board) must work. Because the Control Board Sequencer contains loopback circuitry, attempt to isolate the problem before taking signatures.

4-38. How -The Sequence Pattern Trigger Memories are loaded via the Mainframe Interface and the State Recognition Latch/Counters in the count mode. Also needed for both loading and unloading the Memories (RAMs) is the Sequence State BSS0-3 provided by the Control Board Sequencer. The outputs of the RAMs are OR'd and sent to the Control Board as Sequence Patterns. On the Control Board, PPLS latches the Sequence State at U17, then the Sequence State is read by the Sequence Read Register. During the test, the pipeline strobe PPLS is driven by U5(CTL BD).

4-39. Two signature loops are required. The first checks RAM addresses and inputs, the second checks RAM outputs.

4-40. Results -Sequence Patterns LBSP0-3 are driven by U12 and tested by Loop D.

```
10 MHz State Test: Board in Slot 3        Pass  Tested:  1   Failed:  0

  Slot  3: 20 Channel Acquisition
  Test  3: Sequence Patterns


 Sequence RAMs:          Address  Patterns
                         76543210   3210
 All patterns true                  0000
 All patterns false                 0000

 Data bits:  0 to  3     00000000   0000
             4 to  7     00000000   0000
             8 to 11     00000000   0000
            12 to 15     00000000   0000
            16 to 19     00000000   0000
```

Figure 4-5. Sequence Patterns

4-41. Figure 4-5 Interpretation.

All patterns true	0000
All patterns false	0000

(all patterns true shows that all Acquision boards can release the Sequence Pattern Bus and allow it to float low; the four bits are the output of U12 and all other drivers of LBSP0-3. All patterns false shows that U12 can drive LBSP0-3 high.)

Data bits: 0 to 3	00000000	0000
4 to 7	00000000	0000
8 to 11	00000000	0000
12 to 15	00000000	0000
16 to 19	00000000	0000

(The eight bits of address and four bits of patterns for data bits 0 to 3 are address of U64 and the output of U64 respectively.

Data bits 4 to 7 = U63
8 to 11 = U62
12 to 15 = U61
16 to 19 = U60

4-42. Loop C Signature Path for RAM addresses and inputs: Sequence Pattern RAMs U60-U64, U82, U115, U2, U18 (CTL BD), U42 (CTL BD).

Loop D Signature Path for RAM outputs: U17 (CTL BD), U6 (CTL BD), U12, U50, U65, Sequence Pattern RAMs U60-U64.

4-43. TEST 4: TRACE MEMORY. LOOPS E,F,G,H,I and J

4-44. Trace Memory Read. Loop E

4-45. Purpose - to verify functioning of the Trace Pod Data Memory.

4-46. Control Board Circuitry involved -Strobe Generator which controls the write cycle timing of the Trace Memory. Signals used include PBSTBREQ, PBPLS, HBQWRT, LBMACS. Other control signals from the Control Board are P/NBDSTB, PBRSTB and LBCLR.

4-47. How -Trace Pod Data Memory (Trace Memory) consists of RAMs which recive data through a Pipeline Register and are addressed by means of a Memory Address Counter (MAC) and Memory Address Selector. The RAMs are loaded by means of a write strobe, HBQWRT, which enables both the MAC and the write function of the RAMs. They are unloaded by a read strobe and a RAM selector, U79, through the latch U113. One difficulty in testing this circuit is the data source; it is the State Recognition Latch/Counters. The Counters count synchronously and load identical data into each RAM. Therefore, regardless of which RAM output is selected, the same data appears on the RAM output bus.

4-48. Results - All results are read through latch U113.

4-49. Trace Memory Write. Loops F through J

4-50. Loop F probes the addresses of the Trace Pod Data Memory (U92 - U96) when the Trace Pod Memory Address Counter (U108, U110) is selected by the Trace Pod Data Memory Address Selector (U109, U111).

4-51. Loop F will find address problems that are hidden in the Loop F test. In Loop E, it is possible for the RAM outputs to be bad with all RAM inputs good. However, Loop F catches these problems because it reads the RAMs during the write cycle.

4-52. Loops G through J. If a problem occurs in determining which RAM is degrading the bus, use the additional signature loops, F, G, H, I, and J, which allow for various RAMs to be removed from the board. The additional loops have the same signatures as the primary loop with the exception of RAM outputs and U113.

```
10 MHz State Test: Board in Slot 3        Pass  Tested:  1   Failed:  0

  Slot  3: 20 Channel Acquisition
  Test  4: Trace memory

   (1 = Error)        Address Bit          Data Channel
                        76543210        9876543210987654321O

 Data all zeroes                        00000000000000000000

 Data all ones                          00000000000000000000

 Address test           00000000        00000000000000000000

 Address counter reset    Pass

 Store Qualification      Pass
```

Figure 4-6. Trace Memory

4-53. Figure 4-6 Interpretation.

```
   Data all zeroes              00000000000000000000
   Data all ones                00000000000000000000

      (twenty bit memory, b19 - b16 = U92
                          b15 - b12 = U94
                          b11 -  b8 = U93
                           b7 -  b4 = U96
                           b3 -  b0 = U95)

   Address test  00000000       00000000000000000000

      (eight bit address is output of U109 and U110; output selected
      by LBMACSEL on pin 1)

   Address counter reset:  Pass   (U108 and U110 pin 1)

   Store Qualification:  Pass   (HBQWRT, U13 pin 10)
```

4-54. Loop E Signature Path: U113, U92-U96, U79, U78, U77, U76, U111, U109, U108, U110, U112, U13.

Loop F through Loop J Signature Paths - RAMs as appropriate.

Loop G has U92 removed, Loop H has U92 and U93 removed, etc.

4-55. TEST 5: OVERVIEW EVENT MEMORY. LOOPS K and L

NOTE: See Test 2 for other possible failure modes.

4-56. Overview Event Memory Read. Loop K

4-57. Purpose - to verify the Overview Event Memory System.

4-58. Control Board Circuitry involved -Strobe Generator, Sequencer and Analysis Controller. The signal LBOVEN from the Sequencer is used for the first time. Other signals active are PBSTBREQ, HBOWRT, PBPLS, LBMACS, and LBCLR.

4-59. How -The Event Memory cannot be loaded directly. The data inputs to the Memory are the outputs of the Overview Event/Range Decode Memories. Data is loaded into U16 of the Decode Memory from the Mainframe Interface. Only one location, 00 Hex, is used. That address is provided by the outputs of U18 and U20 of the Decode Memory. Addressing of U18 and U20 is accomplished by holding the Overview State/ Time Counter in a reset state, address is 00 Hex, while the Pod Data TTL/ECL Translators are disabled.

4-60. Interactive read refers to the State Analyzer's ability to read the Event Memories while a trace is in progress. Two monostables U102 go low to prohibit reading during a strobe cycle; during this test the monostables are always sampled high.

4-61. The first part of this test verifies that the Overview Memory Address Counter, Wrap bit (U90 pin 6) and Measurement Complete bit (U90 pin 10) can be cleared, count and overflow. The MAC, Wrap and Measurement Complete can be read directly by the MAC Latches.

4-62. The second part tests the Null Event Decoder which controls the write enable of the RAMs. Then the RAMs are loaded and read via the Event Data Latch.

4-63. Results -all outputs of this test are read at the MAC Latches, U117 and U118, and the Event Data Latch, U119. Interactive read is bits 7 and 8 on latches U118 and U119.

4-64. Overview Event Memory Write. Loop L

4-65. Loop L probes the addresses of the Overview Event Memory (U106, U107, U120 and U121) when the Overview Memory Address Counter (U87, U88, U89) is selected by the Overview Memory Address Selector (U103, U105).

4-66. Loop L will find address problems that are hidden in Loop K. In Loop K it is possible to have RAM outputs bad and all RAM inputs good. This is due to probing the addresses during the read cycle, while Loop L probes the addresses during the write cycle.

```
10 MHz State Test: Board in Slot 3       Pass  Tested:  1   Failed:  0

  Slot  3: 20 Channel Acquisition
  Test  5: Overview event memory

                    10 - valid data flags
 Interactive read   00

                    MW10987654321O - meas. complete, wrap, address
 Store enable       00000000000000
 Address counter    00000000000000
 Wrap control       00000000000000

                    3210 - data bits
 Null detect        0000
 Data path          0000
 RAM test           0000
```

Figure 4-7. Overview Event Memory

4-67. Figure 4-7 Interpretation.

Interactive read 00

(U102 pin 7 msb, U74 pin 6 lsb)

Store enable 00000000000000

(test LBOVEN through U10 pin 14, U74 pin 9, U73 pin 10, U86 pin 10 then to MAC, U87 - U89 pin 2. MSB is U90 pin 10, (HMCOMP), next is U90 pin 6 (LWRAP), then twelve bits of MAC.)
b0 - b3 = U87
b4 - b7 = U88
b8 - b11 = U89)

Address Counter 00000000000000

(test MAC using HBOWRT for clock. Meas. complete, wrap and MAC bits are same as Store enable)

Wrap Control 00000000000000

(test Wrap bit, U90 pin 10, using HMCEN. Meas. complete, wrap and MAC bits are same as Store enable)

Null detect 0000

(test U75, with results read as RAM outputs: b3 = U120
b2 = U121
b1 = U106
b0 = U107)

Data path 0000
RAM test 0000

(test U91 and RAMs, bits are same as Null detect)

4-68. Loop K Signature Path for Store enable, Address counter and Wrap control: U117, U118, U87-U90, U86, U73, U74, U75, U10, U6 (CTL BD), U40 (CTL BD).

Loop K Signature Path for Null detect, Data path and RAM test: U119, U106, U107, U120, U121, U103-U105, U91, U8, U7, U16, U18, U20, U42, U23, U84, U82.

4-69. TEST 6: OVERVIEW/RANGE DECODE RAMs. LOOP M

NOTE: See Test 2 for other possible failure modes.

4-70. Purpose -to verify the Overview Event/Range Decode Memories: U16, U18 and U20.

4-71. Control Board Circuitry involved -Strobe Generator, Sequencer and Analysis Controller. Signals tested for the first time are PBOVRST to reset the Counter and HBOVCQ to enable the Counter. Other signals used are PBSTBREQ, PBSRS, PBPLS, HBOWRT and LBCLR.

4-72. How -The Mainframe writes to the decode RAMs which are addressed by the Overview State Time Counter. The decode RAM outputs are stored in location zero of the Overview Event Memory and then read by the Mainframe. Bits 9 through 19 of the Counter go through an exclusive OR gate which is tested here. Note that the Pod Data ECL/TTL Translators are disabled, and that the Overview Event Memory circuitry was tested in Test 5.

4-73. Results -All results for this test are latched by the Overview Event Pipeline Register, U7, then they pass through the previously tested Overview Event Memory back to the Mainframe Interface.

```
10 MHz State Test: Board in Slot 3        Pass  Tested:  1   Failed:  0

  Slot  3: 20 Channel Acquisition
  Test  6: Overview/Range decode RAMs

                Data Path  Data Storage
                   3210         3210

 10422              0000         0000            (1 = Error)
 10474, upper       0000         0000
 10474, lower       0000         0000

           Count bits: 98765432109

 Exclusive or gate     00000000000
```

Figure 4-8. Overview Range/Decode RAMs

4-74. Figure 4-8 Interpretation.

	Data Path 3210	Data Storage 3210	
10422	0000	0000	(U16)
10474, upper	0000	0000	(U20)
10474, lower	0000	0000	(U18)

(Data Path indicates each data line is intact, Data Storage indicates all memory locations are functioning)

Exclusive or gate 00000000000

(represents the eleven high order bits of the counter fed into U21)

4-75. Loop M Signature Path: U7, U16, U18, U20, U42, U71, U23, U84, U21, U43, U57.

4-76. TEST 7: OVERVIEW/RANGE FUNCTIONS. LOOP N

NOTE: See Test 2 for other possible failure modes.

4-77. Purpose -to allow data from the State Recognition Latch/Counters to address the Overview Event/Range Decode Memory, and to test the Range Patterns, LBRP0-3, and Overview Trigger Enable, HBOTF, circuitry.

4-78. Control Board Circuitry involved -Strobe Generator, Sequencer and Analysis Controller. Range Patterns are received as inputs LRP0-3 by the Analysis Controller that outputs NTRIG. HBOTF is stored as HOTFB in U73(CTL BD). Other signals used are PBSTBREQ, P/NBSRS, PBPLS, PBOVRST, HBOVCQ, HB0WRT, and LBCLR.

4-79. How -The Pod Data TTL/ECL Translators are tested by enabling them and allowing them to address the Overview Event/Range Decode Memory. The Decode Memory is read through the Overview Event Memory by the Mainframe Interface.

4-80. The Range Pattern driver, U4, is tested by sending patterns to the Analysis Controller on the Control Board.

4-81. The Overview Trigger Enable, U43, is tested by sending HBOTF to the Control Board where the Analysis Controller recognizes a trigger by outputting NTRIG.

4-82. Event trigger flag storage is the storing of Overview Trigger Flag, HBOTF, in the Status Memory of the Control Board.

4-83. Results - refer to the interpretation that follows.

```
10 MHz State Test: Board in Slot 3        Pass  Tested:  1   Failed:  0

  Slot  3: 20 Channel Acquisition
  Test  7: Overview/Range functions

                              9876543210 9876543210
 User data to range RAMs  0000000000 0000000000        (1 = Error)

 Range pattern driver                        0000

 Event trigger driver                        0000

 Event trigger flag storage     Pass
```

Figure 4-9. Overview/Range Functions

4-84. Figure 4-9 Interpretation.

User data to range RAMs 0000000000000000000

(twenty bit input which addresses U20 and U18; U23 is reset, U37 -U41 are active; b19 = SYND19 through b1 = SYND0; storage in U20 and U18 previously tested)

Range pattern driver 0000

(four bit output of U4, LBRP0-3; U1(CTL BD) could cause failure)

Event trigger driver 0000

(four bit output of U7 OR'd by U43)

Event trigger flag storage Pass

(Control Board bit tested for first time. U74(CTL BD) HBOTF stored in U73(CTL BD))

4-85. Loop N Signature Path for User data: U18, U20, U37, U41.

Loop N Signature Path for pattern driver: U1(CTL BD), U4, U16.

Loop N Signature Path for trigger driver: U1(CTL BD), U16(CTL BD), U43, U7.

Loop N Signature Path for trigger flag storage: U73(CTL BD), U74(CTL BD), U43, U7.

4-86. TEST 8: STATE COUNT. LOOP O

4-87. Purpose -test Overview State/Time Counter in count states mode.

4-88. Control Board Circuitry Involved -Strobe Generator, Sequencer and Analysis Controller. All SEB signals used have been previously tested; signals are PBSTBREQ, PBSRS, PBPLS, HBOVCQ, PBOVRST, HBWRT, and LBCLR.

4-89. How -The Overview State/Time Counter is made to count states by means of the control register, U71, and the Counter's control inputs. Since most of this circuitry has been previously tested, failure is probably due to the Counter malfunctioning. Check the 25MHz input whenever the Counter is tested because it is needed to clock internal registers even when counting states.

4-90. Results -The Counter outputs control the Decode Memory, which controls storage of data in Event Memory. Event Memory is read by the Mainframe Interface.

4-91. Results -all results are passed through the Event Memory, which is read at the Event Data Latch U119.

```
10 MHz State Test: Board in Slot 3        Pass  Tested:  1   Failed:  0

  Slot  3: 20 Channel Acquisition
  Test  8: State count

                        9876543210987654321O

 Reset                  OOOOOOOOOOOOOOOOOOOO          (1 = Error)

 Count enable                       OOOOOOOO

 20 bit count mode      OOOOOOOOOOOOOOOOOOOO

 Walking ones           OOOOOOOOOOOOOOOOOOOO

 Acq board driving HBWRT                   Pass
```

Figure 4-10. State Count

4-92. Figure 4-10 Interpretation.

Reset 00000000000000000000

(twenty bit counter output controlled by PBOVRST, U23 pin 26)

Count enable 00000000

(test HBOVCQ, U23 pin 32, by reading least significant eight bits of Counter)

20 bit count mode 00000000000000000000

(Counter, U23, clocked by HBOWRT)

Walking ones

(Counter, U23, clocked by HBOWRT)

Acq board driving HBWRT Pass

(Counter, U23, clocked by signal PINC)

4-93. Loop 0 Signature Path: U20, U18, U21, U23, U71, U57, U97.

4-94. TEST 9: OTHER COUNTER TESTS. NO SIGNATURES

4-95. Purpose -test Counter in a count time mode. Also, test prescale function of Counter.

4-96. How -Pin 8, U23, is high to select a count time mode. L25MHZ is used to clock Counter.

4-97. Results -Test takes over 12 seconds. 20 bit patterns are read through the Decode Memory and Event Memory. Failure most likely due to malfunctioning of Counter.

```
10 MHz State Test: Board in Slot 3        Pass  Tested:  1   Failed:  0

  Slot  3: 20 Channel Acquisition
  Test  9: Other counter tests

 Prescale 1  Pass

          2  Pass

          3  Pass

 Time enable Pass

 Time reset  Pass

 Prescale 4  Pass
```

Figure 4-11. Other Counter Tests

4-98. No signatures are available due to length of test.

4-99. DATA PROBE INTERFACE TEST. LOOPS P and Q

4-100. Purpose -test the State Recognition Latch/Counters in latch mode.

4-101. Test Conditions and Operation -to perform this test, either the General Purpose Data Probe (Loop N) or the General Purpose Preprocessor (Loop O) must be connected to the 20 Channel Acquisition board. Run the test using the command "run preprocessor test 1 repeat RETURN". Note that the inputs to the Data Probe or General Purpose Preprocessor must be open.

4-102. How -the DAC (U34) is programmed so that threshold swing at the Data Probe or GP Preprocessor causes a data pattern to be input at the State Recognition Latch/Counters. The signal LLOAD is not asserted, which allows the State Recognition circuit to parallel load data from the probe (LLOAD asserted allows the Latch/Counters to count, and is used while loading the various RAMs before a run).

4-103. Results -The latched data is pipelined to the Trace Pod Data Memories and read by the Mainframe at U113. If test 4, Trace Memory, passes, then failure of this test is due to a faulty data probe, the DAC circuit, or the State Recognition Latch/Counters.

```
10 MHz State Test: Preprocessor          Fail  Tested:  1   Failed:  0

  Preproc: GP Probes
  Test  1: Clock/Data channel verification

                          76543210             76543210
 Clock Edges,  Positive: 00000000  Negative: 00000000  Recommendation:
 Clock Qualifiers, High: 00000000       Low: 00000000    Unhook Probe
                                                         Leads.
 Slot            19     CHANNELS     0
   5     Pod 1:  0000000000000000000
   4     Pod 2:  0000000000000000000     Pod 3:  0000000000000000000
```

Figure 4-12. Data Probe Interface

```
10 MHz State Test: Preprocessor          Pass  Tested:  1   Failed:  0

  Preproc: General Purpose Preprocessor
  Test  1: Clock / Data Channel Verification

                          76543210             76543210
 Clock Edges,  Positive: 00000000  Negative: 00000000
 Clock Qualifiers, High: 00000000       Low: 00000000

 Slot            19     CHANNELS     0
   5     Pod 1:  0000000000000000000
   4     Pod 2:  0000000000000000000     Pod 3:  0000000000000000000
```

Figure 4-13. Data Probe Interface

4-104. Loop P and Q Signature Path: U45-U49, U81, U71, U83, U10, U34.

Board # 64623-66503 **Test 1: Loop A - VH = 7222**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U 34- 2	PU2F	U 99- 1	17CC	U114-12	9A5U
U 34- 3	6U29	U 99- 2	0000	U114-13	P87H
U 34- 4	997U	U 99- 3	6599		
U 34- 5	281H			U115- 1	83C7
U 34- 6	57PP	U100-10	F1H9	U115- 2	U195
U 34- 7	U195	U100-11	C3UC	U115- 3	25FF
U 34- 8	9A5U			U115- 4	57PP
U 34- 9	P9FH	U101- 1	17CC	U115- 5	5A3U
U 34-12	8F89	U101- 2	6599	U115- 6	281H
		U101- 3	0000	U115- 8	997U
U 83- 1	2C7A			U115- 9	PC5H
U 83- 2	9636	U114- 1	17CC	U115-10	6U29
U 83- 3	AC33	U114- 2	6599	U115-11	1H0C
U 83- 4	65P5	U114- 3	5958	U115-12	PU2F
U 83- 5	F3CC	U114- 4	2C7A	U115-13	9H0P
U 83- 6	17CC	U114- 5	P414		
U 83- 7	8F89	U114- 6	9636	U116- 1	F1H9
		U114- 8	AC33	U116- 2	17CC
		U114- 9	H911	U116- 3	C3UC
		U114-10	P9FH		
		U114-11	9CPU		

Board # 64623-66503 **Test 1: Loop A - VH = 7222**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

Control Board Signatures (ICs on Control Board)

U 52- 5 C3UC

Board # 64623-66503 Test 2: Loop B - VH = 9PF7

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U 3- 3	557U	ECL
U 3- 4	9306	ECL
U 3- 5	0HF1	
U 3- 7	FCC8	
U 3-10	A4CF	
U 3-11	CAC6	
U 3-12	3A7C	ECL
U 3-13	2471	ECL
U 10- 2	8AC4	ECL
U 10- 3	1473	ECL
U 10- 4	1473	
U 10- 5	1473	
U 10- 6	8AC4	ECL
U 10- 7	1473	ECL
U 14- 3	4512	ECL
U 14- 4	C0P5	ECL
U 14- 5	2P22	
U 14- 7	HCH5	
U 14-10	3AH3	
U 14-11	0832	
U 14-12	A414	ECL
U 14-13	96U5	ECL

U45 THROUGH U49
COMMON SIGNATURES

PIN 1	HC10
PIN 2	1473
PIN 9	high
PIN 11	41C0
PIN 12	5CAP
PIN 13	3045
PIN 14	50FP

U51 THROUGH U55
COMMON SIGNTURES

PIN 4	83FF
PIN 5	2P22
PIN 6	7266
PIN 7	HCH5
PIN 9	3AH3
PIN 10	47U6
PIN 11	0832
PIN 12	355P
U 51- 1	41C0
U 51- 3	0C2U
U 51-13	50FP
U 51-14	3045
U 51-15	5ACP
U 52- 1	41C0
U 52- 3	8HF7
U 52-13	50FP
U 52-14	3045
U 52-15	5ACP
U 53- 1	41C0
U 53- 3	F702
U 53-13	50FP
U 53-14	3045
U 53-15	5ACP
U 54- 1	41C0
U 54- 3	8390
U 54-13	50FP
U 54-14	3045
U 54-15	5ACP
U 55- 1	41C0
U 55- 3	AHPP
U 55-13	50FP
U 55-14	3045
U 55-15	5ACP

U66 THROUGH U70
COMMON SIGNATURES

PIN 4	PFCA
PIN 5	0HF1
PIN 6	7P09
PIN 7	FCC8
PIN 9	A4CF
PIN 10	AUF2
PIN 11	CAC6
PIN 12	24H0
U 66- 1	41C0
U 66- 3	0C2U
U 66-13	50FP
U 66-14	3045
U 66-15	5ACP
U 67- 1	41C0
U 67- 3	8HF7
U 67-13	50FP
U 67-14	3045
U 67-15	5ACP
U 68- 1	41C0
U 68- 3	F702
U 68-13	50FP
U 68-14	3045
U 68-15	5ACP
U 69- 1	41C0
U 69- 3	8390
U 69-13	50FP
U 69-14	3045
U 69-15	5ACP
U 70- 1	41C0
U 70- 3	AHPP
U 70-13	50FP
U 70-14	3045
U 70-15	5ACP
U 81- 8	HC10
U 81- 9	45H7
U 81-10	HC10
U 81-11	45H7
U 83- 1	4C80
U 83- 2	1536
U 83- 3	275A
U 83- 4	7CP7
U 83- 5	7CP7
U 83- 6	9PF7
TOTLZ	7181
U 83- 7	high

Board # 64623-66503 **Test 2: Loop B - VH = 9PF7**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U 83- 9	high	U114- 8	275A	U115- 6	83FF
U 83-10	HC10	U114- 9	C99H	U115- 8	7266
U 83-11	AHPP	U114-10	PFCA	U115- 9	PFA1
U 83-12	8390	U114-11	727H	U115-10	47U6
U 83-13	F702	U114-12	7P09	U115-11	H931
U 83-14	8HF7	U114-13	P0FP	U115-12	355P
U 83-15	0C2U			U115-13	AC99
		U115- 1	3105		
U114- 3	H547	U115- 2	AUF2	U116- 1	8AC4
U114- 4	4C80	U115- 3	CA17	U116- 2	9PF7
U114- 5	8CU1	U115- 4	24H0	TOTLZ	7181
U114- 6	1536	U115- 5	1H0C	U116- 3	1473

Board # 64623-66503 Test 2: Loop B - VH = 9PF7

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

Control Board Signatures (ICs on Control Board)

U 8- 1	0000		U 24- 9	8AC4	ECL	U 52- 2	1473	ECL
TOTLZ	6016		U 24-12	high	ECL	U 52- 4	high	ECL
U 8- 2	0000		U 24-13	1473	ECL	U 52- 5	1473	
TOTLZ	6016		U 24-15	1473	ECL	U 52-10	high	
U 8- 3	1473							

Board # 64623-66503 **Test 3: Loop C - VH = 6FF8**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U	2- 3	UH20	ECL	PIN	1	P275	U 60-20 PA66
U	2- 4	UH20		PIN	2	CH0F	
U	2- 5	A000		PIN	3	4P1A	U 61-20 H383
U	2- 7	A000	ECL	PIN	4	C6C1	
U	2-11	5UCP	ECL	PIN	5	A000	U 62-20 5A5A
U	2-12	5UCP		PIN	6	5UCP	
U	2-13	U8FH		PIN	7	U8FH	U 63-20 2C98
U	2-15	U8FH	ECL	PIN	9	47PC	
				PIN	11	A22H	U 64-20 82A7
U60 THROUGH U64				PIN	13	C7F6	
COMMON SIGNATURES				PIN	15	369U	
				PIN	21	UH20	

Board # 64623-66503 Test 3: Loop C - VH = 6FF8

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

Control Board Signatures (ICs on Control Board)

U 18- 2	0000	ECL	U 18-12	0000	ECL	U 42- 7	6FF8	ECL
TOTLZ	1291		TOTLZ	6004		TOTLZ	4486	
U 18- 3	0000	ECL	U 18-13	0000	ECL	U 42- 8	6FF8	ECL
TOTLZ	1291		TOTLZ	2908		TOTLZ	3651	
U 18- 4	6FF8	ECL	U 18-14	0000	ECL	U 42-18	6FF8	ECL
U 18- 7	UH20	ECL	TOTLZ	1291		TOTLZ	3161	
U 18- 9	A000	ECL	U 18-15	0000	ECL	U 42-19	6FF8	ECL
U 18-10	5UCP	ECL	TOTLZ	1291		TOTLZ	5172	
U 18-11	U8FH	ECL						
			U 42- 6	6FF8	ECL			
			TOTLZ	4167				

Board # 64623-66503 **Test 3: Loop D - VH = 6FF8**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U 12- 3	34HF	ECL	U 60-10	8601		U 63-14	3161
U 12- 4	640H	ECL	U 60-12	F823		U 63-16	1P03
U 12- 5	08F5		U 60-14	9FA5			
U 12- 7	5814		U 60-16	2F1A		U 64-10	4462
U 12-10	A48C					U 64-12	8U7F
U 12-11	7526		U 61-10	3UFH		U 64-14	C181
U 12-12	F843	ECL	U 61-12	25A8		U 64-16	U98A
U 12-13	C8FC	ECL	U 61-14	F8HH			
			U 61-16	4FPF		U 65- 1	8U7F
U 50- 1	U98A					U 65- 2	3F9U
U 50- 2	1P03		U 62-10	61P9		U 65- 3	4786
U 50- 3	P372		U 62-12	4786		U 65- 4	4462
U 50- 4	C181		U 62-14	P044		U 65- 5	7526
U 50- 5	08F5		U 62-16	P372		U 65- 6	A48C
U 50- 6	5814					U 65- 8	5404
U 50- 8	3161		U 63-10	5404		U 65- 9	61P9
U 50- 9	P044		U 63-12	3F9U		U 65-10	3UFH
U 50-10	F8HH					U 65-11	8601
U 50-11	9FA5					U 65-12	25A8
U 50-12	4FPF					U 65-13	F823
U 50-13	2F1A						

Board # 64623-66503 **Test 3: Loop D - VH = 6FF8**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

Control Board Signatures (ICs on Control Board)

U	6-11	F843	ECL	U	17- 7	640H	ECL	U	17-11	low ECL
U	6-14	C8FC	ECL	U	17- 9	34HF	ECL			
				U	17-10	C8FC	ECL			

Board # 64623-66503 Test 3: BONUS LOOP - VH = FA8U

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - U99-3 Cntl. Bd.
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

Control Board Signatures (ICs on Control Board)

U 17- 2	16C5	ECL	U 17-11	low	ECL	U 83-11	9C87	ECL
U 17- 3	900U	ECL	U 17-12	80U3	ECL	U 83-15	low	ECL
U 17- 4	high	ECL	U 17-13	U899	ECL			
U 17- 5	U82F	ECL	U 17-14	low	ECL	U 84- 3	6114	ECL
U 17- 6	32A3	ECL	U 17-15	9C87	ECL	U 84- 7	9F53	ECL
U 17- 7	AA23	ECL				U 84-11	6677	ECL
U 17- 9	0CA0	ECL	U 83- 3	900U	ECL	U 84-15	PP96	ECL
U 17-10	AAFP	ECL	U 83- 7	16C5	ECL			

Board # 64623-66503 Test 4: Loop E - VH = UUPO

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U 13- 3	UUP0	ECL
U 13- 4	UUP0	
TOTLZ	9753	
U 13- 5	UUP0	
TOTLZ	3850	
U 13- 6	0000	ECL
U 13- 7	UUP0	ECL
U 13-10	0000	ECL
U 13-12	UUP0	
TOTLZ	0770	
U 13-13	0000	
TOTLZ	0775	
U 13-15	0000	ECL
U 76- 2	UP56	
U 76- 3	F050	
U 76- 4	F3A9	
U 76- 5	F8UA	
U 76- 6	FU16	
U 76- 7	F3A9	
U 76- 8	2270	
U 76- 9	2FAU	
U 76-11	0000	
TOTLZ	0775	
U 77- 2	UP56	
U 77- 3	F050	
U 77- 4	F3A9	
U 77- 5	F8UA	
U 77- 6	FU16	
U 77- 7	F3A9	
U 77- 8	2270	
U 77- 9	2FAU	
U 77-11	0000	
TOTLZ	0775	
U 77-12	2FAU	
U 77-13	2270	
U 77-14	F3A9	
U 77-15	FU16	
U 77-16	F8UA	
U 77-17	F3A9	
U 77-18	F050	
U 77-19	UP56	

U 78- 2	UP56
U 78- 3	F050
U 78- 4	F3A9
U 78- 5	F8UA
U 78- 6	FU16
U 78- 7	F3A9
U 78- 8	2270
U 78- 9	2FAU
U 78-11	0000
U 78-12	2FAU
U 78-13	2270
U 78-14	F3A9
U 78-15	FU16
U 78-16	F8UA
U 78-17	F3A9
U 78-18	F050
U 78-19	UP56
U 79- 1	P2A9
U 79- 2	0000
TOTLZ	OFLO
U 79- 3	P2A9
U 79- 4	UUP0
TOTLZ	0775
U 79-11	1H70
U 79-12	FH0F
U 79-13	46H2
U 79-14	8H85
U 79-15	1C2C
U 81- 5	0000
TOTLZ	3850
U 81- 6	UUP0
TOTLZ	3850

U92 THROUGH U96
COMMON SIGNATURES

PIN 1	3AFC
PIN 2	H6A5
PIN 3	0C42
PIN 4	13F6
PIN 5	3707
PIN 6	H8C1
PIN 7	A907
PIN 9	2FAU
PIN 10	88U1
PIN 11	FU16
PIN 12	3186
PIN 13	F8UA
PIN 14	A935
PIN 15	UP56
PIN 16	109P
PIN 20	UUP0
TOTLZ	0770
PIN 21	U0H6
U 92-18	1H70
U 93-18	46H2
U 94-18	FH0F
U 95-18	1C2C
U 96-18	8H85
U 98- 8	P2A9
U 98- 9	high
U 98-10	1H49
U 98-11	UUP0
TOTLZ	4620
U 99-11	P2A9
U 99-12	0000
TOTLZ	OFLO
U 99-13	1H49
U100- 5	1H49
U100- 6	P2A9
U108- 1	UUP0
TOTLZ	0006
U108- 2	UUP0
TOTLZ	0770
U108-11	7C95
U108-12	F2F7

Board # 64623-66503 **Test 4: Loop E - VH = UUPO**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U108-13	FA22
U108-14	5P67
U108-15	1H91
U109- 1	UUPO
TOTLZ	9753
U109- 2	5P67
U109- 3	56P7
U109- 4	A907
U109- 5	FA22
U109- 6	2751
U109- 7	H8C1
U109- 9	3707
U109-10	F8P7
U109-11	F2F7
U109-12	U0H6
U109-13	0U36
U109-14	7C95
U110- 1	UUPO
TOTLZ	0006
U110- 2	UUPO
TOTLZ	0770
U110- 7	1H91
U110-10	1H91
U110-11	9217
U110-12	H0F8
U110-13	6211
U110-14	0C70

U111- 1	UUPO
TOTLZ	9753
U111- 2	0C70
U111- 3	F52C
U111- 4	3AFC
U111- 5	6211
U111- 6	2945
U111- 7	H6A5
U111- 9	0C42
U111-10	U4A2
U111-11	H0F8
U111-12	13F6
U111-13	PF26
U111-14	9217
U112- 2	56P7
U112- 3	1H49
U112- 4	UUPO
U112- 5	2751
U112- 6	F8P7
U112- 7	UUPO
TOTLZ	OFLO
U112- 8	UUPO
TOTLZ	OFLO
U112- 9	0U36
U112-11	0000
TOTLZ	3850
U112-12	F52C
U112-13	UUPO
TOTLZ	OFLO
U112-14	UUPO

TOTLZ	OFLO
U112-15	2945
U112-16	U4A2
U112-17	UUPO
TOTLZ	OFLO
U112-18	1H49
U112-19	PF26
U113- 1	P2A9
U113- 2	162U
U113- 3	109P
U113- 4	A935
U113- 5	2U94
U113- 6	3737
U113- 7	3186
U113- 8	88U1
U113- 9	825P
U113-11	UUPO
TOTLZ	3850
U113-12	162U
U113-13	109P
U113-14	A935
U113-15	2U94
U113-16	3737
U113-17	3186
U113-18	88U1
U113-19	825P
TP3	UUPO
TOTLZ	4620

Board # 64623-66503 **Test 4: Loop E - VH = UUPO**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

Control Board Signatures (ICs on Control Board)

U 5- 3	0000	ECL	U 5-15	UUP0	ECL	U 19- 2	0000	ECL
TOTLZ	0075		TOTLZ	9753		TOTLZ	3850	
U 5- 6	0000	ECL				U 19- 3	UUP0	ECL
TOTLZ	9753		U 8- 8	0000		TOTLZ	3850	
U 5- 7	7UU0	ECL	TOTLZ	0006		U 19- 4	UUP0	ECL
U 5-10	0000	ECL	U 8- 9	UUP0		TOTLZ	3850	
TOTLZ	9753		TOTLZ	0006		U 19- 5	UUP0	ECL
U 5-11	7CUA	ECL	U 8-10	UUP0		TOTLZ	13603	
U 5-12	UUP0	ECL	TOTLZ	0006		U 19- 6	0000	ECL
TOTLZ	9753		U 8-11	UUP0		TOTLZ	3850	
U 5-13	UUP0	ECL	TOTLZ	0006		U 19- 7	0000	ECL
TOTLZ	9753		U 8-12	0000		TOTLZ	3850	
U 5-14	0000	ECL	TOTLZ	0006				
TOTLZ	0770		U 8-13	0000				
			TOTLZ	0006				

Board # 64623-66503 **Test 4: Loop F - VH = 5U91**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - U96-20
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U 92- 1	6297	U 94-15	HC58	U108-11	3C64
U 92- 2	7P7A	U 94-18	1658	U108-12	8H2C
U 92- 3	0F39	U 94-20	5U91	U108-13	C985
U 92- 4	7676	TOTLZ	0770	U108-14	FA8U
U 92- 5	H2CA	U 94-21	64U5	U108-15	470A
U 92- 6	P614				
U 92- 7	951P	U 95- 1	6297	U109- 1	0000
U 92- 9	2H5U	U 95- 2	7P7A	TOTLZ	9753
U 92-11	43C1	U 95- 3	0F39	U109- 2	FA8U
U 92-13	3545	U 95- 4	7676	U109- 3	1658
U 92-15	HC58	U 95- 5	H2CA	U109- 4	951P
U 92-18	49F9	U 95- 6	P614	U109- 5	C985
U 92-20	5U91	U 95- 7	951P	U109- 6	1658
TOTLZ	0770	U 95- 9	2H5U	U109- 9	H2CA
U 92-21	64U5	U 95-11	43C1	U109-10	1658
		U 95-13	3545	U109-11	8H2C
U 93- 1	6297	U 95-15	HC58	U109-12	64U5
U 93- 2	7P7A	U 95-18	5U91	U109-13	1658
U 93- 3	0F39	TOTLZ	0770	U109-14	3C64
U 93- 4	7676	U 95-20	5U91		
U 93- 5	H2CA	TOTLZ	0770	U110- 1	5U91
U 93- 6	P614	U 95-21	64U5	TOTLZ	0006
U 93- 7	951P			U110- 2	5U91
U 93- 8	low	U 96- 1	6297	TOTLZ	0770
U 93- 9	2H5U	U 96- 2	7P7A	U110- 7	470A
U 93-11	43C1	U 96- 3	0F39	U110-10	470A
U 93-13	3545	U 96- 4	7676	U110-11	29P7
U 93-15	HC58	U 96- 5	H2CA	U110-12	53A8
U 93-18	5U91	U 96- 6	P614	U110-13	21PC
TOTLZ	0770	U 96- 7	951P	U110-14	3H06
U 93-20	5U91	U 96- 9	2H5U		
TOTLZ	0770	U 96-11	43C1	U111- 1	0000
U 93-21	64U5	U 96-13	3545	TOTLZ	9753
		U 96-15	HC58	U111- 2	3H06
U 94- 1	6297	U 96-18	5U91	U111- 3	1658
U 94- 2	7P7A	TOTLZ	0770	U111- 4	6297
U 94- 3	0F39	U 96-20	5U91	U111- 5	21PC
U 94- 4	7676	TOTLZ	0770	U111- 6	1658
U 94- 5	H2CA	U 96-21	64U5	U111- 9	0F39
U 94- 6	P614			U111-10	1658
U 94- 7	951P	U108- 1	5U91	U111-11	53A8
U 94- 9	2H5U	TOTLZ	0006	U111-12	7676
U 94-11	43C1	U108- 2	5U91	U111-13	1658
U 94-13	3545	TOTLZ	0770	U111-14	29P7

Board # 64623-66503 **Test 4: Loop G - VH = UUPO**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

Remove RAM U92.

U93 THROUGH U96
COMMON SIGNATURES

PIN 10 88U1
PIN 12 3186
PIN 14 A935
PIN 16 109P

NOTE: Signatures for RAM addresses and inputs are the same as Loop E.

Board # 64623-66503 **Test 4: Loop H - VH = UUPO**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

Remove RAMs U92 and U93.

U94 THROUGH U96
COMMON SIGNATURES

PIN 10 88U1
PIN 12 3186
PIN 14 A935
PIN 16 109P

NOTE: Signatures for RAM addresses and inputs are the same as Loop E.

Board # 64623-66503 **Test 4: Loop I - VH = UUPO**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

Remove RAMs U92 through U94.

U95 THROUGH U96
COMMON SIGNATURES

PIN 10 P694
PIN 12 C196
PIN 14 A935
PIN 16 7PUC

NOTE: Signatures for RAM addresses and inputs are the same as Loop E.

Board # 64623-66503 **Test 4: Loop J - VH = UUPO**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

Remove RAMs U92 through U95

U 96-10 734A
U 96-12 58HC
U 96-14 H48A
U 96-16 3U7H

NOTE: Signatures for RAM addresses and inputs are the same as Loop E.

Board # 64623-66503 Test 5: Loop K - VH = OP5U

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U 7- 2	high	ECL	U 16-19	72P7	ECL	U 42- 1	6C62	ECL
U 7- 3	high	ECL	U 16-21	A711	ECL	U 42- 2	P4H0	ECL
U 7- 4	88H8	ECL	U 16-23	7U14	ECL	U 42- 5	P4H0	
U 7- 5	A711	ECL				U 42- 7	6C62	
U 7- 6	7U14	ECL	U 18- 2	CPCA	ECL	U 42-10	CC9U	
U 7- 7	7U14	ECL	U 18- 3	CPCA	ECL	U 42-11	72P7	
U 7- 9	0000	ECL	U 18- 4	low	ECL	U 42-14	72P7	ECL
TOTLZ	24598		U 18- 5	low	ECL	U 42-15	CC9U	ECL
U 7-10	A711	ECL	U 18- 6	low	ECL			
U 7-11	5CP3	ECL	U 18- 7	low	ECL	U 71- 1	high	
U 7-12	2A47	ECL	U 18- 8	low	ECL	U 71- 2	A92F	
U 7-13	6U8A	ECL	U 18- 9	low	ECL	U 71- 3	6C62	
U 7-14	71A8	ECL	U 18-11	low	ECL	U 71- 4	P4H0	
U 7-15	0PPU	ECL	U 18-13	low	ECL	U 71- 5	low	
			U 18-14	low	ECL	U 71- 6	low	
U 8- 3	0PPU	ECL	U 18-15	8970	ECL	U 71- 7	CC9U	
U 8- 4	0PPU		U 18-16	P6F8	ECL	U 71- 8	HP4C	
U 8- 5	71A8		U 18-18	6C62	ECL	U 71- 9	high	
U 8- 7	71A8	ECL	U 18-19	P4H0	ECL	U 71-11	12H1	
U 8-11	6U8A	ECL	U 18-20	CC9U	ECL	U 71-12	low	
U 8-12	6U8A		U 18-21	72P7	ECL	U 71-13	F311	
U 8-13	88H8		U 18-22	CPCA	ECL	U 71-14	6F6F	
U 8-15	88H8	ECL	U 18-23	CPCA	ECL	U 71-15	2586	
						U 71-16	low	
U 10-11	0000	ECL	U 20- 2	6U94	ECL	U 71-17	72P7	
U 10-12	0000		U 20- 3	6U94	ECL	U 71-18	A33F	
TOTLZ	24598		U 20- 4	low	ECL	U 71-19	8970	
U 10-13	8C0P		U 20- 5	low	ECL			
U 10-14	8551	ECL	U 20- 6	low	ECL	U 73- 8	CH48	
			U 20- 7	low	ECL	U 73- 9	high	
U 16- 2	2A47	ECL	U 20- 8	low	ECL	U 73-10	C317	
U 16- 4	5CP3	ECL	U 20- 9	low	ECL	U 73-11	0000	
U 16- 6	6C62	ECL	U 20-11	low	ECL	TOTLZ	24599	
U 16- 7	P4H0	ECL	U 20-13	low	ECL	U 73-12	0P5U	
U 16- 8	8UA6	ECL	U 20-14	low	ECL	TOTLZ	24599	
U 16- 9	6U94	ECL	U 20-15	low	ECL	U 73-13	0P5U	
U 16-10	6U94	ECL	U 20-16	HU71	ECL			
U 16-11	6U94	ECL	U 20-18	6C62	ECL	U 74- 1	0000	
U 16-13	CPCA	ECL	U 20-19	P4H0	ECL	TOTLZ	24599	
U 16-14	CPCA	ECL	U 20-20	CC9U	ECL	U 74- 2	8C0P	
U 16-15	CPCA	ECL	U 20-21	72P7	ECL	U 74- 4	9FFF	
U 16-16	CPCA	ECL	U 20-22	6U94	ECL	U 74- 5	AA8A	
U 16-17	6U94	ECL	U 20-23	6U94	ECL	U 74- 6	0P5U	
U 16-18	CC9U	ECL						

Board # 64623-66503 **Test 5: Loop K - VH = OP5U**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

TOTLZ	24593	
U 74- 8	C317	
U 74- 9	8C0P	
U 74-10	9FFF	
U 74-12	AA8A	
U 74-13	high	
U 75- 1	88H8	
U 75- 2	6U8A	
U 75- 3	71A8	
U 75- 4	0PPU	
U 75- 5	A92F	
U 75- 8	AA8A	
U 82- 1	98U5	
U 82- 2	9C78	
U 82- 3	PA4P	
U 82- 4	069U	
U 82- 5	287U	
U 82- 6	FA22	
U 82- 7	HU71	
U 82- 9	P6F8	
U 82-10	8UA6	
U 83- 1	98U5	
U 83- 2	9C78	
U 83- 3	PA4P	
U 83- 4	069U	
U 83- 5	4AFP	
U 83- 6	FA22	
U 83- 9	12H1	
U 84- 1	P6F8	ECL
U 84- 7	P6F8	
U 84-10	HU71	
U 84-11	8UA6	
U 84-14	8UA6	ECL
U 84-15	HU71	ECL
U 86- 1	2586	
U 86- 2	3142	
U 86- 3	F865	
U 86- 4	high	
U 86- 5	0P5U	
U 86- 6	0000	
TOTLZ	24593	
U 86- 8	0P5U	
TOTLZ	24593	
U 86- 9	0000	
U 86-10	CH48	
U 86-11	0P5U	
TOTLZ	24593	
U 86-12	0000	
U 86-13	high	
U 87- 1	0P5U	
TOTLZ	0028	
U 87- 2	0P5U	
TOTLZ	24593	
U 87- 7	9FFF	
U 87-10	9FFF	
U 87-11	C16A	
U 87-12	A021	
U 87-13	1U9F	
U 87-14	63F7	
U 87-15	1HA6	
U 88- 1	0P5U	
TOTLZ	0028	
U 88- 2	0P5U	
TOTLZ	24593	
U 88- 7	1HA6	
U 88-10	1HA6	
U 88-11	PC7P	
U 88-12	4H50	
U 88-13	6968	
U 88-14	U49H	
U 88-15	2787	
U 89- 1	0P5U	
TOTLZ	0028	
U 89- 2	0P5U	
TOTLZ	24593	
U 89- 7	2787	
U 89-10	2787	
U 89-11	PPA0	
U 89-12	PA60	
U 89-13	F645	
U 89-14	P282	
U 89-15	3142	
U 90- 1	0P5U	
TOTLZ	0028	
U 90- 2	3142	
U 90- 4	0P5U	
U 90- 6	3821	
U 90-10	9FFF	
U 90-11	0P5U	
TOTLZ	0028	
U 90-12	0P5U	
U 90-13	F865	
U 91- 2	0PPU	
TOTLZ	1917	
U 91- 4	0PPU	
TOTLZ	1917	
U 91- 5	71A8	
U 91- 7	71A8	
U 91- 9	0000	
TOTLZ	24598	
U 91-10	6U8A	
U 91-12	6U8A	
U 91-13	88H8	
U 91-15	88H8	
U 99-11	FA22	
U 99-12	6358	
U 99-13	A725	
U100- 5	A725	
U100- 6	A97A	
U100- 8	6H07	
U100- 9	6358	
U101-11	FA22	
U101-12	F6AA	
U101-13	6358	
U102- 5	C317	
U102- 7	0P5U	
TOTLZ	25107	
U102- 9	0P5U	

Board # 64623-66503 Test 5: Loop K - VH = OP5U

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

TOTLZ	24599
U102-11	0P5U
TOTLZ	24599
U103- 1	0P5U
TOTLZ	24593
U103- 2	C16A
U103- 3	287U
U103- 4	2620
U103- 5	A021
U103- 6	P411
U103- 7	PA4P
U103- 9	9C78
U103-10	9527
U103-11	1U9F
U103-12	98U5
U103-13	96AA
U103-14	63F7
U104- 1	0P5U
TOTLZ	24593
U104- 2	PC7P
U104- 3	26H1
U104- 4	288P
U104- 5	4H50
U104- 6	17A8
U104- 7	19U7
U104- 9	AF76
U104-10	A229
U104-11	6968
U104-12	4491
U104-13	4AFP
U104-14	U49H
U105- 1	0P5U
TOTLZ	24593
U105- 2	PPA0
U105- 3	069U
U105- 4	08F0
U105- 5	PA60
U105- 6	F9H4
U105- 7	F78C
U105- 9	UC43
U105-10	U51F
U105-11	F645
U105-12	H72H
U105-13	H972
U105-14	P282
U106, U107,	
U120, U121	
COMMON SIGNATURES	
PIN 1	98U5
PIN 2	9C78
PIN 3	PA4P
PIN 4	2620
PIN 5	4491
PIN 6	AF76
PIN 8	0P5U
TOTLZ	0FL0
PIN 12	08F0
PIN 13	F78C
PIN 14	UC43
PIN 15	H72H
PIN 16	288P
PIN 17	19U7
U106- 7	173F
U106-11	6U8A
U107- 7	7202
U107-11	88H8
U117- 1	6H07
U117- 2	653H
U117- 3	63F7
U117- 4	1U9F
U117- 5	PA8U
U117- 6	C5F0
U117- 7	A021
U117- 8	C16A
U117- 9	7FC8
U117-11	6H07
U117-12	FH4P
U117-13	U49H
U117-14	6968
U117-15	6233
U117-16	AH63
U117-17	4H50
U117-18	PC7P
U117-19	H014
U118- 1	6H07
U118- 2	8P2A
U118- 3	P282
U118- 4	F645
U118- 5	5421
U118- 6	9U40
U118- 7	PA60
U118- 8	PPA0
U118- 9	P78U
U118-11	6H07
U118-12	7UFH
U118-13	3821
U118-14	9FFF
U118-15	7UH1
U118-16	0P5U
U118-17	0P5U
U118-18	0P5U
TOTLZ	25107
U118-19	0P5U
U119- 1	A97A
U119- 2	8P2A
U119- 3	H64C
U119- 4	U240
U119- 5	5421
U119- 6	9U40
U119- 7	173F
U119- 8	7202
U119- 9	P78U
U119-11	A97A
U119-12	7UFH
U119-15	7UH1
U119-16	0P5U
U119-17	0P5U
TOTLZ	24593
U119-18	0P5U
U119-19	0P5U
U120- 7	H64C
U120-11	0PPU

Board # 64623-66503 **Test 5: Loop K - VH = OP5U**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U121- 7 U240
U121-11 71A8

Board # 64623-66503 **Test 5: Loop K - VH = OP5U**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

Control Board Signatures (ICs on Control Board)

U 5- 2	0000	ECL	U 8- 9	0P5U			U 40- 8	0P5U	ECL		
TOTLZ	24598		TOTLZ	0028			TOTLZ	0512			
U 5- 3	0000	ECL	U 8-10	0P5U			U 40- 9	AUH1	ECL		
TOTLZ	24598		TOTLZ	0028			U 40-10	998U	ECL		
U 5- 4	0000	ECL	U 8-11	0P5U			U 40-11	51H2	ECL		
TOTLZ	24598		TOTLZ	0028			U 40-13	PH95	ECL		
U 5- 5	61FC	ECL	U 8-12	0000			U 40-14	53FH	ECL		
U 5- 6	0000	ECL	TOTLZ	0028			U 40-15	58F1	ECL		
TOTLZ	24599		U 8-13	0000			U 40-16	9246	ECL		
U 5- 7	61FC	ECL	TOTLZ	0028			U 40-17	9463	ECL		
							U 40-18	0P5U	ECL		
U 6- 9	8551	ECL	U 40- 2	0P5U	ECL		TOTLZ	0290			
U 6-12	0000	ECL	TOTLZ	0512			U 40-19	0P5U	ECL		
TOTLZ	24599		U 40- 4	0P5U	ECL		TOTLZ	0546			
U 6-13	8551	ECL	TOTLZ	0512			U 40-21	8551	ECL		
			U 40- 6	high	ECL		U 40-23	low	ECL		
U 8- 8	0000		U 40- 7	high	ECL						
TOTLZ	0028										

Board # 64623-66503 **Test 5: Loop L - VH = PP8C**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - U86-9
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U 73- 8	45HP	U 88- 2	PP8C	U104- 7	0A8H
U 73- 9	high	TOTLZ	24593	U104- 9	92UH
U 73-10	AC55	U 88- 7	PF93	U104-10	9376
		U 88- 9	high	U104-11	9040
U 74- 1	PP8C	U 88-10	PF93	U104-12	2CPA
TOTLZ	24599	U 88-11	FU09	U104-13	258U
U 74- 2	1HH1	U 88-12	175F	U104-14	A471
U 74- 4	5AC2	U 88-13	9040		
U 74- 5	02CH	U 88-14	A471	U105- 1	AC55
U 74- 6	AC55	U 88-15	33H9	U105- 2	0145
U 74- 8	AC55			U105- 3	0000
U 74- 9	1HH1	U 89- 1	PP8C	TOTLZ	OFLO
U 74-10	5AC2	TOTLZ	0028	U105- 4	PUFP
U 74-12	02CH	U 89- 2	PP8C	U105- 5	CP84
U 74-13	high	TOTLZ	24593	U105- 6	PP8C
		U 89- 7	33H9	U105- 7	UC5A
U 75- 1	657A	U 89- 9	high	U105- 9	4AFF
U 75- 2	P096	U 89-10	33H9	U105-10	0000
U 75- 3	0570	U 89-11	0145	TOTLZ	OFLO
U 75- 4	0605	U 89-12	CP84	U105-11	A447
U 75- 5	2654	U 89-13	A447	U105-12	003F
U 75- 8	02CH	U 89-14	PPC7	U105-13	0000
		U 89-15	HP8C	TOTLZ	OFLO
U 86- 8	PP8C			U105-14	PPC7
TOTLZ	24593	U103- 1	AC55		
U 86- 9	0000	U103- 2	H548	U106- 1	2938
TOTLZ	24598	U103- 3	465U	U106- 2	HF7P
U 86-10	45HP	U103- 4	02HF	U106- 3	88UA
		U103- 5	81F3	U106- 4	02HF
U 87- 1	PP8C	U103- 6	79F4	U106- 5	2CPA
TOTLZ	0028	U103- 7	88UA	U106- 6	92UH
U 87- 2	PP8C	U103- 9	HF7P	U106- 8	PP8C
TOTLZ	24593	U103-10	4636	TOTLZ	OFLO
U 87- 7	5AC2	U103-11	86FF	U106-11	U04C
U 87- 9	high	U103-12	2938	U106-12	PUFP
U 87-10	5AC2	U103-13	4FP7	U106-13	UC5A
U 87-11	H548	U103-14	8C54	U106-14	4AFF
U 87-12	81F3			U106-15	003F
U 87-13	86FF	U104- 1	AC55	U106-16	66P1
U 87-14	8C54	U104- 2	FU09	U106-17	0A8H
U 87-15	PF93	U104- 3	A655		
		U104- 4	66P1	U107- 1	2938
U 88- 1	PP8C	U104- 5	175F	U107- 2	HF7P
TOTLZ	0028	U104- 6	56U3	U107- 3	88UA

Board # 64623-66503 Test 5: Loop L - VH = PP8C

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - U86-9
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U107- 4	02HF	U120- 3	88UA	U121- 3	88UA
U107- 5	2CPA	U120- 4	02HF	U121- 4	02HF
U107- 6	92UH	U120- 5	2CPA	U121- 5	2CPA
U107- 8	PP8C	U120- 6	92UH	U121- 6	92UH
TOTLZ	OFLO	U120- 8	PP8C	U121- 8	PP8C
U107-11	32CH	TOTLZ	OFLO	TOTLZ	OFLO
U107-12	PUFP	U120-11	8302	U121-11	02C8
U107-13	UC5A	U120-12	PUFP	U121-12	PUFP
U107-14	4AFF	U120-13	UC5A	U121-13	UC5A
U107-15	003F	U120-14	4AFF	U121-14	4AFF
U107-16	66P1	U120-15	003F	U121-15	003F
U107-17	0A8H	U120-16	66P1	U121-16	66P1
		U120-17	0A8H	U121-17	0A8H
U120- 1	2938				
U120- 2	HF7P	U121- 1	2938		
		U121- 2	HF7P		

Board # 64623-66503 **Test 6: Loop M - VH = C262**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U 7- 2	2161	ECL	U 18- 8	1U69	ECL	U 21-13	508F	ECL
U 7- 3	2161	ECL	U 18- 9	3H1F	ECL	U 21-14	034H	ECL
U 7- 4	HCHC	ECL	U 18-11	3U8C	ECL	U 21-15	2C76	ECL
U 7- 5	CPU0	ECL	U 18-13	F489	ECL			
U 7- 6	5419	ECL	U 18-14	306U	ECL	U 23- 2	04P7	ECL
U 7- 7	5419	ECL	U 18-15	747U	ECL	U 23- 3	F3C7	ECL
U 7- 9	0000	ECL	U 18-16	P19U	ECL	U 23- 4	214C	ECL
TOTLZ	21100		U 18-18	5UC9	ECL	U 23- 5	P778	ECL
U 7-10	CPU0	ECL	U 18-19	A4P6	ECL	U 23- 6	4H14	ECL
U 7-11	70CU	ECL	U 18-20	68A6	ECL	U 23- 7	low	
U 7-12	89PH	ECL	U 18-21	PF04	ECL	U 23- 8	low	
U 7-13	56H4	ECL	U 18-22	F245	ECL	U 23- 9	H884	
U 7-14	2456	ECL	U 18-23	6P7U	ECL	U 23-14	0FPA	ECL
U 7-15	7212	ECL				U 23-15	H060	ECL
			U 20- 2	4110	ECL	U 23-16	A8PC	ECL
U 8- 3	7212	ECL	U 20- 3	F7FA	ECL	U 23-17	PF5F	ECL
U 8- 7	2456	ECL	U 20- 4	034H	ECL	U 23-18	1U69	ECL
U 8-11	56H4	ECL	U 20- 5	508F	ECL	U 23-19	3H1F	ECL
U 8-15	HCHC	ECL	U 20- 6	A758	ECL	U 23-20	3U8C	ECL
			U 20- 7	A1U2	ECL	U 23-21	F489	ECL
U 16- 2	89PH	ECL	U 20- 8	6257	ECL	U 23-22	306U	ECL
U 16- 4	70CU	ECL	U 20- 9	04P7	ECL	U 23-23	2C76	ECL
U 16- 6	5UC9	ECL	U 20-11	F3C7	ECL	U 23-25	7FFP	ECL
U 16- 7	A4P6	ECL	U 20-13	214C	ECL	U 23-26	A346	ECL
U 16- 8	3F9F	ECL	U 20-14	P778	ECL	U 23-27	0000	ECL
U 16- 9	C335	ECL	U 20-15	4H14	ECL	TOTLZ	20299	
U 16-10	4110	ECL	U 20-16	C100	ECL	U 23-32	370F	ECL
U 16-11	F7FA	ECL	U 20-18	5UC9	ECL	U 23-36	034H	ECL
U 16-13	F245	ECL	U 20-19	A4P6	ECL	U 23-37	508F	ECL
U 16-14	6P7U	ECL	U 20-20	68A6	ECL	U 23-38	A758	ECL
U 16-15	A43F	ECL	U 20-21	PF04	ECL	U 23-39	A1U2	ECL
U 16-16	AH66	ECL	U 20-22	UPAA	ECL	U 23-40	6257	ECL
U 16-17	UPAA	ECL	U 20-23	C335	ECL			
U 16-18	68A6	ECL				U 37- 6	low	
U 16-19	PF04	ECL	U 21- 2	3AHC	ECL			
U 16-21	CPU0	ECL	U 21- 3	6AP6	ECL	U 38- 6	low	
U 16-23	5419	ECL	U 21- 4	4H14	ECL			
			U 21- 5	P778	ECL	U 39- 6	low	
U 18- 2	A43F	ECL	U 21- 6	214C	ECL			
U 18- 3	AH66	ECL	U 21- 7	F3C7	ECL	U 40- 6	low	
U 18- 4	0FPA	ECL	U 21- 9	04P7	ECL			
U 18- 5	H060	ECL	U 21-10	6257	ECL	U 41- 6	low	
U 18- 6	A8PC	ECL	U 21-11	A1U2	ECL			
U 18- 7	PF5F	ECL	U 21-12	A758	ECL			

Board # 64623-66503 Test 6: Loop M - VH = C262

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U 42- 1	5UC9	ECL	U 71- 6	H931		U 97- 3	high	
U 42- 2	A4P6	ECL	U 71- 7	68A6		U 97- 4	C262	
U 42- 5	A4P6		U 71- 8	7H73		TOTLZ	OFLO	
U 42- 7	5UC9		U 71- 9	6C53		U 97- 5	0000	
U 42-10	68A6		U 71-11	661A		TOTLZ	OFLO	
U 42-11	PF04		U 71-12	low		U 97- 7	low	
U 42-14	PF04	ECL	U 71-13	35P4				
U 42-15	68A6	ECL	U 71-14	0H40		U 98- 1	high	
			U 71-15	low		U 98- 2	0000	
U 43- 2	747U	ECL	U 71-16	low		TOTLZ	OFLO	
U 43- 9	low	ECL	U 71-17	PF04		U 98-12	high	
U 43-10	6AP6	ECL	U 71-18	4351		U 98-13	0A19	
U 43-11	2C76	ECL	U 71-19	H884				
U 43-12	low	ECL				U106- 1	35P7	
U 43-13	H884	ECL	U 82- 1	35P7		U106- 2	3F9F	
U 43-14	3AHC	ECL	U 82- 2	3F9F		U106- 3	C262	
U 43-15	747U	ECL	U 82- 3	C262		TOTLZ	OFLO	
			TOTLZ	OFLO		U106- 4	661A	
U 57- 1	low	ECL	U 82- 4	0000		U106- 5	6F03	
U 57- 2	0000	ECL	TOTLZ	OFLO		U106- 6	C87C	
TOTLZ	20299		U 82- 5	H478		U106- 7	989A	
U 57- 5	low		U 82- 6	0A19		U106- 8	C262	
U 57- 7	low		U 82- 7	C100		TOTLZ	OFLO	
U 57-10	H884		U 82- 9	P19U		U106-10	low	
U 57-11	H931		U 82-10	3F9F		U106-11	56H4	
U 57-12	6AP6	ECL				U106-12	C262	
U 57-13	2161	ECL	U 84- 1	P19U	ECL	TOTLZ	0591	
U 57-15	H884	ECL	U 84- 7	P19U		U106-13	C87C	
			U 84-10	C100		U106-14	C87C	
U 58- 3	C262	ECL	U 84-11	3F9F		U106-15	C87C	
TOTLZ	21100		U 84-14	3F9F	ECL	U106-16	C87C	
U 58- 7	0000	ECL	U 84-15	C100	ECL	U106-17	C87C	
TOTLZ	21100							
U 58-12	7FFP	ECL	U 91- 2	7212		U107- 1	35P7	
U 58-13	C262	ECL	U 91- 4	7212		U107- 2	3F9F	
TOTLZ	21100		U 91- 5	2456		U107- 3	C262	
U 58-14	0000	ECL	U 91- 7	2456		TOTLZ	OFLO	
TOTLZ	20299		U 91- 9	0000		U107- 4	661A	
			TOTLZ	21100		U107- 5	6F03	
U 71- 1	high		U 91-10	56H4		U107- 6	C87C	
U 71- 2	low		U 91-11	P4C6		U107- 7	5270	
U 71- 3	5UC9		U 91-12	56H4		U107- 8	C262	
U 71- 4	A4P6		U 91-13	HCHC		TOTLZ	21100	
U 71- 5	low		U 91-15	HCHC				

Board # 64623-66503 **Test 6: Loop M - VH = C262**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U107-10	low	U120- 6	C87C	TOTLZ	OFLO
U107-11	HCHC	U120- 7	81FH	U121- 4	661A
U107-12	C262	U120- 8	C262	U121- 5	6F03
TOTLZ	0303	TOTLZ	21100	U121- 6	C87C
U107-13	C87C	U120-10	low	U121- 7	HA12
U107-14	C87C	U120-11	7212	U121- 8	C262
U107-15	C87C	U120-12	C262	TOTLZ	21100
U107-16	C87C	TOTLZ	2177	U121-10	low
U107-17	C87C	U120-13	C87C	U121-11	2456
		U120-14	C87C	U121-12	C262
U120- 1	35P7	U120-15	C87C	TOTLZ	1158
U120- 2	3F9F	U120-16	C87C	U121-13	C87C
U120- 3	C262	U120-17	C87C	U121-14	C87C
TOTLZ	OFLO			U121-15	C87C
U120- 4	661A	U121- 1	35P7	U121-16	C87C
U120- 5	6F03	U121- 2	3F9F	U121-17	C87C
		U121- 3	C262		

Board # 64623-66503 Test 6: Loop M - VH = C262

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

Control Board Signatures (ICs on Control Board)

U 1- 2	2P27	ECL
U 1- 3	0000	ECL
TOTLZ	21103	
U 1- 4	269F	ECL
U 1- 7	FPAF	ECL
U 1- 8	PF98	ECL
U 1- 9	PF98	ECL
U 1-12	PF98	ECL
U 1-16	0000	ECL
TOTLZ	21103	
U 1-17	7866	
U 1-18	6AP6	
U 1-19	high	
U 1-20	C262	
U 1-21	low	ECL
U 1-30	C262	ECL
TOTLZ	8960	
U 1-33	0000	ECL
TOTLZ	21103	
U 1-34	6C52	
U 1-35	C262	
TOTLZ	5966	
U 1-36	C262	ECL
TOTLZ	8960	
U 1-37	C262	ECL
TOTLZ	8960	
U 1-38	C262	ECL
TOTLZ	8960	
U 1-39	370F	ECL
U 1-40	low	ECL
U 6- 3	7FFP	ECL
U 6- 6	FPAF	ECL
U 6- 7	0000	ECL
TOTLZ	21103	
U 6- 9	0000	ECL
TOTLZ	21358	
U 6-12	0000	ECL
TOTLZ	21103	
U 6-13	low	ECL
U 24- 9	1124	ECL
U 24-12	H884	ECL
U 24-13	F9A0	ECL
U 24-15	A346	ECL
U 40- 2	C262	ECL
TOTLZ	8960	
U 40- 4	C262	ECL
TOTLZ	8960	
U 40- 6	C262	ECL
TOTLZ	9008	
U 40- 7	C262	ECL
TOTLZ	4896	
U 40- 8	C262	ECL
TOTLZ	8960	
U 40- 9	8997	ECL
U 40-10	534F	ECL
U 40-11	49C4	ECL
U 40-13	F168	ECL
U 40-14	60UA	ECL
U 40-15	P7CP	ECL
U 40-16	A24F	ECL
U 40-17	61C8	ECL
U 40-18	C262	ECL
TOTLZ	17968	
U 40-19	C262	ECL
TOTLZ	4896	
U 40-21	low	ECL
U 40-23	FPAF	ECL

Board # 64623-66503 **Test 7: Loop N - VH = 843H**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U 4- 2	19UU	ECL	U 16-15	23P8	ECL	U 20-20	4FAC	ECL
U 4- 3	4PCC	ECL	U 16-16	4707	ECL	U 20-21	365H	ECL
U 4- 4	A76U	ECL	U 16-17	379P	ECL	U 20-22	379P	ECL
U 4- 6	843H	ECL	U 16-18	4FAC	ECL	U 20-23	4C84	ECL
U 4- 7	50PC	ECL	U 16-19	365H	ECL			
U 4-10	PH4A	ECL	U 16-21	PH4A	ECL	U 21- 2	AP0U	ECL
U 4-12	9A6H	ECL	U 16-23	H2HH	ECL	U 21- 3	low	ECL
U 4-13	H2HH	ECL				U 21- 4	666A	ECL
U 4-14	U31A	ECL	U 18- 2	23P8	ECL	U 21- 5	43C3	ECL
U 4-15	272H	ECL	U 18- 3	4707	ECL	U 21- 6	507F	ECL
			U 18- 4	961H	ECL	U 21- 7	C7HU	ECL
U 7- 2	PUH3	ECL	U 18- 5	C42F	ECL	U 21- 9	HA95	ECL
U 7- 3	PUH3	ECL	U 18- 6	4945	ECL	U 21-10	H13P	ECL
U 7- 4	85CA	ECL	U 18- 7	CU0C	ECL	U 21-11	2P83	ECL
U 7- 5	PH4A	ECL	U 18- 8	9AA4	ECL	U 21-12	02HU	ECL
U 7- 6	H2HH	ECL	U 18- 9	4C1H	ECL	U 21-13	25A4	ECL
U 7- 7	H2HH	ECL	U 18-11	UF45	ECL	U 21-14	HH87	ECL
U 7- 9	0000	ECL	U 18-13	F1U4	ECL	U 21-15	C3A1	ECL
U 7-10	PH4A	ECL	U 18-14	0829	ECL			
U 7-11	50PC	ECL	U 18-15	4032	ECL	U 23- 2	HA95	ECL
U 7-12	A76U	ECL	U 18-16	6H0F	ECL	U 23- 3	C7HU	ECL
U 7-13	F731	ECL	U 18-18	C67F	ECL	U 23- 4	507F	ECL
U 7-14	C510	ECL	U 18-19	A4CH	ECL	U 23- 5	43C3	ECL
U 7-15	2U5P	ECL	U 18-20	4FAC	ECL	U 23- 6	666A	ECL
			U 18-21	365H	ECL	U 23- 7	4935	
U 8- 3	2U5P	ECL	U 18-22	37CC	ECL	U 23- 8	low	
U 8- 4	2U5P		U 18-23	AA0U	ECL	U 23- 9	high	
U 8- 5	C510					U 23-14	961H	ECL
U 8- 7	C510	ECL	U 20- 2	HHAA	ECL	U 23-15	C42F	ECL
U 8-11	F731	ECL	U 20- 3	32FU	ECL	U 23-16	4945	ECL
U 8-12	F731		U 20- 4	HH87	ECL	U 23-17	CU0C	ECL
U 8-13	85CA		U 20- 5	25A4	ECL	U 23-18	9AA4	ECL
U 8-15	85CA	ECL	U 20- 6	02HU	ECL	U 23-19	4C1H	ECL
			U 20- 7	2P83	ECL	U 23-20	UF45	ECL
U 16- 2	A76U	ECL	U 20- 8	H13P	ECL	U 23-21	F1U4	ECL
U 16- 4	50PC	ECL	U 20- 9	HA95	ECL	U 23-22	0829	ECL
U 16- 6	C67F	ECL	U 20-10	low	ECL	U 23-23	C3A1	ECL
U 16- 7	A4CH	ECL	U 20-11	C7HU	ECL	U 23-25	F00A	ECL
U 16- 8	947U	ECL	U 20-13	507F	ECL	U 23-26	3C05	ECL
U 16- 9	4C84	ECL	U 20-14	43C3	ECL	U 23-27	0000	ECL
U 16-10	HHAA	ECL	U 20-15	666A	ECL	U 23-32	H415	ECL
U 16-11	32FU	ECL	U 20-16	2048	ECL	U 23-36	HH87	ECL
U 16-13	37CC	ECL	U 20-18	C67F	ECL	U 23-37	25A4	ECL
U 16-14	AA0U	ECL	U 20-19	A4CH	ECL	U 23-38	02HU	ECL

Board # 64623-66503 Test 7: Loop N - VH = 843H

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U 23-39	2P83	ECL	U 41- 1	507F	ECL	U 57-10	high	
U 23-40	H13P	ECL	U 41- 2	C7HU	ECL	U 57-11	1P50	
			U 41- 5	H438		U 57-12	low	ECL
U 37- 1	C42F	ECL	U 41- 6	4935		U 57-13	PUH3	ECL
U 37- 2	961H	ECL	U 41- 7	UP7U		U 57-15	high	ECL
U 37- 5	H438		U 41-10	P812				
U 37- 6	4935		U 41-11	704P		U 58- 3	843H	ECL
U 37- 7	UP7U		U 41-14	666A	ECL	TOTLZ	8074	
U 37-10	P812		U 41-15	43C3	ECL	U 58- 7	0000	ECL
U 37-11	704P					TOTLZ	8074	
U 37-14	CU0C	ECL	U 43- 2	4032	ECL	U 58-12	F00A	ECL
U 37-15	4945	ECL	U 43- 3	9U35	ECL	U 58-13	843H	ECL
			U 43- 4	C510	ECL	TOTLZ	8074	
U 38- 1	4C1H	ECL	U 43- 5	2U5P	ECL	U 58-14	0000	ECL
U 38- 2	9AA4	ECL	U 43- 6	PUH3	ECL	TOTLZ	6910	
U 38- 5	H438		U 43- 7	9P70	ECL			
U 38- 6	4935		U 43- 9	4935	ECL	U 71- 1	high	
U 38- 7	UP7U		U 43-10	low	ECL	U 71- 2	low	
U 38-10	P812		U 43-11	C3A1	ECL	U 71- 3	C67F	
U 38-11	704P		U 43-12	4935	ECL	U 71- 4	A4CH	
U 38-14	F1U4	ECL	U 43-13	high	ECL	U 71- 5	4935	
U 38-15	UF45	ECL	U 43-14	AP0U	ECL	U 71- 6	1P50	
			U 43-15	4032	ECL	U 71- 7	4FAC	
U 39- 1	4032	ECL				U 71- 8	C85C	
U 39- 2	0829	ECL	U 56- 2	4935		U 71- 9	9A6H	
U 39- 5	H438		U 56- 3	4935		U 71-11	5A01	
U 39- 6	4935		U 56- 4	4935		U 71-12	low	
U 39- 7	UP7U		U 56- 5	4935		U 71-13	3AA6	
U 39-10	P812		U 56- 6	4935		U 71-14	C5FC	
U 39-11	704P		U 56- 7	4935		U 71-15	low	
U 39-14	25A4	ECL	U 56- 9	4935		U 71-16	low	
U 39-15	HH87	ECL	U 56-10	4935		U 71-17	365H	
			U 56-11	4935		U 71-18	9FF2	
U 40- 1	2P83	ECL	U 56-12	4935		U 71-19	high	
U 40- 2	02HU	ECL	U 56-13	9A6H				
U 40- 5	H438		U 56-14	9A6H		U 84- 7	6H0F	
U 40- 6	4935		U 56-15	low		U 84-10	2048	
U 40- 7	UP7U					U 84-11	947U	
U 40-10	P812		U 57- 1	4935	ECL			
U 40-11	704P		U 57- 2	0000	ECL	U 91- 2	2U5P	
U 40-14	HA95	ECL	TOTLZ	6910		U 91- 4	2U5P	
U 40-15	H13P	ECL	U 57- 5	low		U 91- 5	C510	
			U 57- 7	4935		U 91- 7	C510	
			U 57- 9	high		U 91- 9	0000	

Board # 64623-66503 **Test 7: Loop N - VH = 843H**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

TOTLZ	8074
U 91-10	F731
U 91-12	F731
U 91-13	85CA
U 91-15	85CA
U 97- 3	high
U 97- 4	843H
TOTLZ	OFLO
U 97- 5	0000
TOTLZ	OFLO
U 97- 7	low
U 98- 1	high
U 98- 2	0000
TOTLZ	OFLO
U 98-12	high
U 98-13	FH56
U106- 1	C330
U106- 2	HA13
U106- 3	843H
TOTLZ	OFLO
U106- 4	146H
U106- 5	H93C
U106- 6	496C
U106- 7	9U52
U106- 8	843H
TOTLZ	OFLO
U106-10	low
U106-11	F731
U106-12	843H
TOTLZ	0484
U106-13	496C
U106-14	496C
U106-15	496C
U106-16	496C
U106-17	496C
U107- 1	C330
U107- 2	HA13
U107- 3	843H
TOTLZ	OFLO
U107- 4	146H
U107- 5	H93C
U107- 6	496C
U107- 7	118F
U107- 8	843H
U107-10	low
U107-11	85CA
U107-12	843H
TOTLZ	OFLO
U107-13	496C
U107-14	496C
U107-15	496C
U107-16	496C
U107-17	496C
U119- 1	FH56
U119- 2	H16A
U119- 3	7408
U119- 4	CFP5
U119- 5	1987
U119- 6	3A30
U119- 7	9U52
U119- 8	118F
U119- 9	C4PP
U120- 1	C330
U120- 2	HA13
U120- 3	843H
TOTLZ	OFLO
U120- 4	146H
U120- 5	H93C
U120- 6	496C
U120- 7	7408
U120- 8	843H
TOTLZ	OFLO
U120-10	low
U120-11	2U5P
U120-12	843H
TOTLZ	1053
U120-13	496C
U120-14	496C
U120-15	496C
U120-16	496C
U120-17	496C
U121- 1	C330
U121- 2	HA13
U121- 3	843H
TOTLZ	OFLO
U121- 4	146H
U121- 5	H93C
U121- 6	496C
U121- 7	CFP5
U121- 8	843H
TOTLZ	OFLO
U121-10	low
U121-11	C510
U121-12	843H
TOTLZ	0661
U121-13	496C
U121-14	496C
U121-15	496C
U121-16	496C
U121-17	496C

Board # 64623-66503 **Test 7: Loop N - VH = 843H**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

Control Board Signatures (ICs on Control Board)

U 1- 4	HFF9	ECL	U 6- 7	0000	ECL	U 40-18	843H	ECL
U 1- 5	0000	ECL	TOTLZ	8093		TOTLZ	10751	
TOTLZ	0190					U 40-19	843H	ECL
U 1- 6	0000	ECL	U 16- 2	9U35	ECL	TOTLZ	4648	
TOTLZ	0269		U 16- 5	9U35	ECL	U 40-21	9P70	ECL
U 1- 7	HA47	ECL				U 40-23	4437	ECL
U 1- 8	FU0F	ECL	U 24- 9	CU38	ECL			
U 1- 9	P849	ECL	U 24-12	08HF	ECL	U 73- 1	68PH	
U 1-12	P849	ECL	U 24-13	C7P4	ECL	U 73- 2	68PH	
U 1-15	U31A	ECL	U 24-15	3C05	ECL	U 73- 3	68PH	
U 1-17	F554					U 73- 4	68PH	
U 1-21	low	ECL	U 40- 2	843H	ECL	U 73- 5	68PH	
U 1-22	low	ECL	TOTLZ	4096		U 73- 6	68PH	
U 1-23	low	ECL	U 40- 4	843H	ECL	U 73- 7	68PH	
U 1-24	low	ECL	TOTLZ	4096		U 73-10	PFH0	
U 1-25	272H	ECL	U 40- 6	843H	ECL	U 73-11	FU0F	
U 1-27	low	ECL	TOTLZ	5752		U 73-12	PFH0	
U 1-28	19UU	ECL	U 40- 7	843H	ECL	U 73-13	high	
U 1-29	4PCC	ECL	TOTLZ	5296		U 73-14	PFH0	
U 1-35	843H		U 40- 8	843H	ECL	U 73-15	1C08	
TOTLZ	3306		TOTLZ	4096		U 73-16	PFH1	
U 1-36	843H	ECL	U 40- 9	364H	ECL	U 73-18	68PH	
TOTLZ	4096		U 40-10	C13A	ECL	U 73-20	843H	
U 1-37	843H	ECL	U 40-11	54FF	ECL	TOTLZ	0659	
TOTLZ	4096		U 40-13	P16U	ECL	U 73-21	68PH	
			U 40-14	048H	ECL			
U 6- 3	F00A	ECL	U 40-15	HUF1	ECL	U 74-13	1C08	
U 6- 6	4437	ECL	U 40-16	A218	ECL	U 74-14	9U35	ECL
			U 40-17	246H	ECL			

Board # 64623-66503 **Test 8: Loop O - VH = F5H9**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U 21- 2	7UP4	ECL	U 23-18	H403	ECL	U 71- 9	2735	
U 21- 3	C313	ECL	U 23-19	C300	ECL	U 71-11	2443	
U 21- 4	9438	ECL	U 23-20	P9AC	ECL	U 71-12	low	
U 21- 5	4998	ECL	U 23-21	A318	ECL	U 71-13	6U7F	
U 21- 6	FUP8	ECL	U 23-22	2568	ECL	U 71-14	46UF	
U 21- 7	855C	ECL	U 23-23	CC07	ECL	U 71-15	low	
U 21- 9	HUU0	ECL	U 23-25	5A7P	ECL	U 71-16	low	
U 21-10	659A	ECL	U 23-26	A27U	ECL	U 71-17	U595	
U 21-11	6FFH	ECL	U 23-27	0000	ECL	U 71-18	525P	
U 21-12	CAPC	ECL	U 23-32	H602	ECL	U 71-19	76FA	
U 21-13	600A	ECL	U 23-36	PFA5	ECL			
U 21-14	PFA5	ECL	U 23-40	659A	ECL	U 97- 2	low	
U 21-15	CC07	ECL				U 97- 3	AA84	
			U 57- 2	0000	ECL	U 97- 4	F5H9	
U 23- 2	HUU0	ECL	TOTLZ	14642		TOTLZ	OFLO	
U 23- 3	855C	ECL	U 57- 5	0000		U 97- 5	0000	
U 23- 4	FUP8	ECL	TOTLZ	0055		TOTLZ	OFLO	
U 23- 5	4998	ECL				U 97- 6	F5H9	
U 23- 6	9438	ECL	U 71- 1	high		TOTLZ	0055	
U 23- 7	low		U 71- 2	low		U 97- 7	0000	
U 23- 8	low		U 71- 3	F991		TOTLZ	0055	
U 23- 9	76FA		U 71- 4	9U04				
U 23-14	PFA5	ECL	U 71- 5	low		U 98- 1	high	
U 23-15	0FUA	ECL	U 71- 6	P2PF		U 98- 2	6U5H	
U 23-16	H61C	ECL	U 71- 7	89H5		U 98-12	AA84	
U 23-17	003H	ECL	U 71- 8	01P2		U 98-13	AACF	

Board # 64623-66503 Probes Test: Loop P - VH = 3U9F

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

Connect General Purpose Probes, Model 64635A, to J3 and J4 cables.
Run the test "run preprocessor test 1 repeat".
5005A setup unchanged.

U 10- 2	0000	ECL
U 10- 3	3U9F	ECL
U 10- 4	3U9F	
TOTLZ	0041	
U 10- 5	3U9F	
TOTLZ	0041	
U 34- 2	3UF3	
U 34- 3	1UH1	
U 34- 4	1UH1	
U 34- 5	1UH1	
U 34- 6	0UH8	
U 34- 7	0UH8	
U 34- 8	0UH8	
U 34- 9	0UH8	
U 34-12	1U8P	
U 45- 1	high	
U 45- 2	3U9F	
TOTLZ	0041	
U 45- 3	206H	
U 45- 4	206H	
U 45- 5	206H	
U 45- 6	206H	
U 45- 9	low	
U 45-11	001U	
U 45-12	001U	
U 45-13	001U	
U 45-14	001U	
U 46- 1	high	
U 46- 2	3U9F	
TOTLZ	0041	
U 46- 3	206H	
U 46- 4	206H	
U 46- 5	206H	
U 46- 6	206H	

U 46- 9	low
U 46-11	001U
U 46-12	001U
U 46-13	001U
U 46-14	001U
U 47- 1	high
U 47- 2	3U9F
TOTLZ	0041
U 47- 3	206H
U 47- 4	206H
U 47- 5	206H
U 47- 6	206H
U 47- 9	low
U 47-11	001U
U 47-12	001U
U 47-13	001U
U 47-14	001U
U 48- 1	high
U 48- 2	3U9F
TOTLZ	0041
U 48- 3	206H
U 48- 4	206H
U 48- 5	206H
U 48- 6	206H
U 48- 9	low
U 48-11	001U
U 48-12	001U
U 48-13	001U
U 48-14	001U
U 49- 1	high
U 49- 2	3U9F
TOTLZ	0041
U 49- 3	206H
U 49- 4	206H
U 49- 5	206H

U 49- 6	206H
U 49- 9	low
U 49-11	001U
U 49-12	001U
U 49-13	001U
U 49-14	001U
U 71- 1	high
U 71-11	2U95
U 71-12	high
U 71-13	1UH1
U 81- 1	high
U 81- 2	low
U 81- 3	high
U 81- 4	low
U 81- 5	0000
TOTLZ	0010
U 81- 6	3U9F
TOTLZ	0010
U 81- 8	high
U 81- 9	low
U 81-10	high
U 81-11	low
U 81-12	low
U 81-13	high
U 83- 1	2012
U 83- 2	301C
U 83- 3	301C
U 83- 4	0U87
U 83- 5	0U87
U 83- 6	301C
U 83- 7	1U8P
U 83-10	high
TP 1	206H

Board # 64623-66503 **Preprocessor Test: Loop Q - VH = 3395**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
------	Start - Positive	Data - Low **	Qual/Stop - LMAP2
------	Stop - Negative	Clock - TTL	Clock - TP3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

Plug J3 cable into POD 1 of the Preprocessor.
Remove all user inputs to the Preprocessor.
Run the test "run preprocessor test 1 repeat".
5005A setup unchanged.

U 10- 4 3395
U 10- 5 3395

U25, U27,U29,
U31 and U33
COMMON SIGNATURES

PIN 2	3U7F	ECL
PIN 3	0FP9	ECL
PIN 4	0FP9	
PIN 5	0FP9	
PIN 6	3U7F	ECL
PIN 7	0FP9	ECL
PIN 10	3U7F	ECL
PIN 11	0FP9	ECL
PIN 12	0FP9	
PIN 13	0FP9	
PIN 14	3U7F	ECL
PIN 15	0FP9	ECL

U 34- 2 H903
U 34- 3 7A1A
U 34- 4 7A1A
U 34- 5 7A1A
U 34- 6 2C96
U 34- 7 2C96
U 34- 8 2C96
U 34- 9 2C96
U 34-12 908F

U45 THROUGH U49
COMMON SIGNATURES

PIN 1	high
PIN 2	3395
TOTLZ	0048
PIN 3	0FP9
PIN 4	0FP9
PIN 5	0FP9
PIN 6	0FP9
PIN 9	low
PIN 11	U399
PIN 12	U399
PIN 13	U399
PIN 14	U399

U 71- 1 high
U 71-11 6219
U 71-12 high
U 71-13 7A1A

U 81- 1 high
U 81- 2 low
U 81- 3 high
U 81- 4 low
U 81- 8 high
U 81- 9 low
U 81- 10 high
U 81- 11 low
U 81- 12 low
U 81- 13 high

U 83- 1 A319
U 83- 2 U295
U 83- 3 U295
U 83- 4 F100
U 83- 5 F100
U 83- 6 U295
U 83- 7 908F
U 83- 10 high

TP1 529H

SECTION V

ADJUSTMENTS

5-1. INTRODUCTION.

5-2. This section describes adjustments and checks required to return the instrument to peak operating capability after repairs have been made.

5-3. SAFETY REQUIREMENTS.

5-4. Although this instrument has been designed in accordance with international safety standards, general safety precautions must be observed during all phases of operation, service, and repair of the instrument. Failure to comply with precautions listed in the Safety Summary at the front of this manual or with specific warnings given throughout the manual could result in serious injury or death or damage to equipment. Service adjustments should be performed only by qualified service personnel.

5-5. EQUIPMENT REQUIRED.

5-6. 4 1/2 Digit Voltmeter with +/-1 mV accuracy. (Hewlett-Packard Model 3466A or equilivant.)

5-7. PROCEDURE.

5-8. This procedure assumes that all other modules of this system are working properly, and all are calibrated and meet or exceed their respective specifications.

NOTE

Installation and removal of PC Boards must be done with the A.C. Power for the Mainframe turned off.

5-9. THRESHOLD ADJUSTMENTS.

a. Acquisition Board adjustments may be made with or without the Control Board installed in the Mainframe.

b. Place the 20 Channel Acquisition Board on an extender board. The IMB and SEB Bus Cables do not need to be connected.

c. If it is not already disconnected, disconnect the Data Probe Cable from J3.

d. Connect the ground lead of the DMM to TP5, GND. See figure 5-1.

e. Connect the positive lead of the DMM to Testpoint 1.

f. Press opt_test , press RETURN . The display will indicate the option modules present and the card slot number they are located in.

g. Press "slot number", RETURN .

"Slot number" is a number from 0 to 9 equal to the location of the 20 Channel ACQ Board.

h. Press run , "slot number" , test , 10 , RETURN . The CRT should now display "Test 10: Threshold Circuit Calibration".

i. Each time the RETURN key is pressed, the D/A Converter will be set to a new value. Press RETURN until "Reference = -4.267 V Negative Limit" is displayed.

j. Adjust -FS, R2, to -4.267 V +/-1 mV. See Figure 5-1.

k. Continue pressing RETURN until "Reference = +433 mV ECL (-1.3 V)" is displayed.

l. Adjust +FS, R1, to +433 mV +/-1 mV. See Figure 5-1.

m. Each time RETURN is pressed, the D/A Converter will be set to a different value. Press RETURN six times and verify that the value measured on the DMM is within +/-33 mV of the value displayed for all six DAC levels. (If the voltages are not correct, there is most likely a problem in the DAC and must be corrected using the Performance Verification.)

n. Press end , RETURN , end to exit the 20 Channel Acquisition Performance Verification.

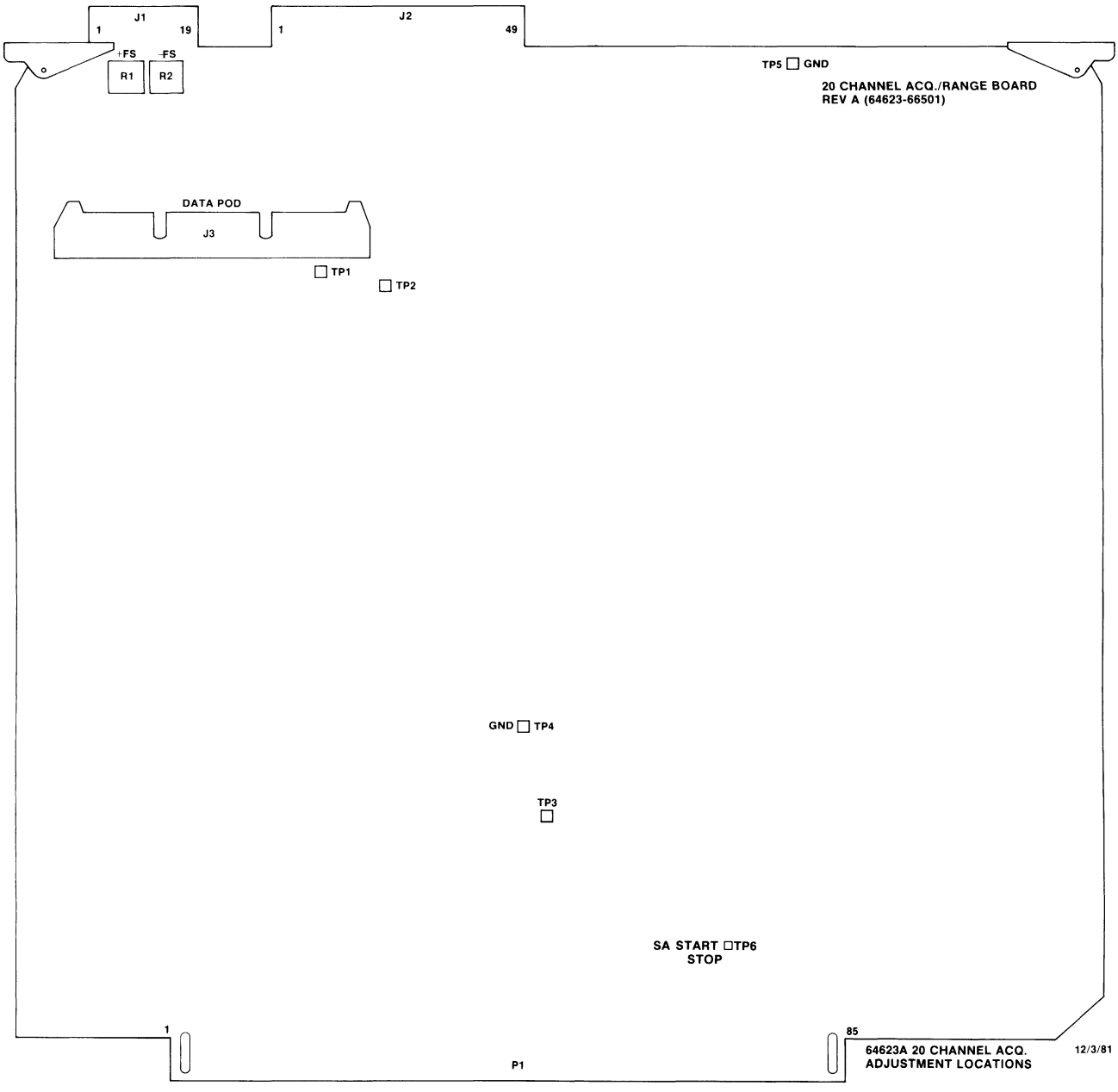


Figure 5-1. Adjustment Locations

NOTES

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts list and throughout the manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturers' five-digit code numbers.

6-3. ABBREVIATIONS.

6-4. Table 6-1 lists abbreviations used in the parts list, the schematics and throughout the manual. In some cases, two forms of the abbreviation are used: one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lowercase and uppercase letters.

6-5. REPLACEABLE PARTS LIST.

6-6. Table 6-2 is the list of replaceable parts and is organized as follows:

a. Chassis-mounted parts in alphanumerical order by reference designation.

b. Electrical assemblies and their components in alphanumerical order by reference designation.

c. Miscellaneous parts.

The information given for each part consists of the following:

a. The Hewlett-Packard part number and the check digit.

b. The total quantity (Qty) in the instrument.

c. The description of the part.

d. A five-digit code that indicates the manufacturer.

e. The manufacturers' part number.

The total quantity for each part is given only once - at the first appearance of the part number in the list.

6-7. ORDERING INFORMATION.

6-8. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard office.

6-9. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument repair number, the description and function of

the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

6-10. SPARE PARTS KIT.

6-11. A spare parts kit is not available at this time.

6-12. DIRECT MAIL ORDER SYSTEM.

6-13. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No Maximum or minimum on any mail order (there is a minimum order amount, for parts ordered through a local HP office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices -to provide these advantages, a check or money order must accompany each order.

6-14. Mail-order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are located at the back of this manual.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without

Table 6-2. Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	64623A		1	20 CHANNEL STATE DATA ACQUISITION	28480	64623A
A1	64623-66503	9	1	20 CHANNEL STATE DATA ACQUISITION BOARD	28480	64623-66503
A1C1	0160-5321	8	50	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C2	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C3	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C4	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C5	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C6	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C7	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C8	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C9	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C10	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C11	0160-3508	9	1	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A1C12	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C13	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C14	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C15	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C16	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C17	0160-0178	3	2	CAPACITOR-FXD 27PF +-5% 300VDC MICA	28480	0160-0178
A1C18	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C19	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C20	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C21	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C22	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C23	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C24	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C25	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C26	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C27	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C28	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C29	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C30	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C31	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C32	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C33	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C34	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C35	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C36	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C37	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C38	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C39	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C40	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C41	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C42	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C43	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C44	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C45	0160-0205	7	1	CAPACITOR-FXD 10PF +-5% 500VDC MICA	28480	0160-0205
A1C46	0160-0178	3		CAPACITOR-FXD 27PF +-5% 300VDC MICA	28480	0160-0178
A1C47	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C48	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C49	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C50	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C51	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C52	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C53	0180-1746	5	3	CAPACITOR-FXD 150UF+-10% 20VDC TA	56289	150D156X9020B2
A1C54	0180-1746	5		CAPACITOR-FXD 150UF+-10% 20VDC TA	56289	150D156X9020B2
A1C55	0180-1746	5		CAPACITOR-FXD 150UF+-10% 20VDC TA	56289	150D156X9020B2
A1C56	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-5321
A1C57	0160-5321	8		CAPACITOR-FXD .01UF +80-20% 100VDC	28480	0160-5321
A1J3	1251-6651	3	1	CONNECTOR 50-PIN M POST TYPE	28480	1251-6651
A1MP1	64623-85001	2	1	EXTRACTOR-P.C. BOARD	28480	64623-85001
A1MP2	64623-85002	3	1	EXTRACTOR-P.C. BOARD	28480	64623-85002
A1MP3	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
A1MP4	1480-0116	8		PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
A1R1	2100-3982	9	2	RESISTOR-TRMR 500 10% CCP SIDE-ADJ	28480	2100-3982
A1R2	2100-3982	9		RESISTOR-TRMR 500 10% CCP SIDE-ADJ	28480	2100-3982
A1R3	0757-0394	0	3	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A1R4	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A1R5	0757-0430	5	1	RESISTOR 2.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2211-F

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A1R6	0757-0437	2	1	RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4751-F
A1R7	0757-0431	6	2	RESISTOR 2.43K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2431-F
A1R8	0757-0431	6		RESISTOR 2.43K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2431-F
A1R9	0757-0410	1	2	RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A1R10	0757-0280	3	4	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R11	0698-3153	9	1	RESISTOR 3.83K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3831-F
A1R12	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R13	0757-0438	3	1	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1R14	0698-3152	8	1	RESISTOR 3.48K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3481-F
A1R15	0698-3154	0	1	RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A1R16	0757-0283	6	3	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A1R17	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A1R18	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R19	0757-0410	1		RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A1R20	0757-0442	9	10	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R21	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R22	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R23	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R24	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R25	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R26	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R27	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R28	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R29	0757-0449	6	2	RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
A1R30	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A1R31	0757-0449	6		RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
A1R32	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R33	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A1R34	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1TP1	0360-0535	0	5	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1U1	1820-2359	7	2	IC MISC ECL 14-INP	07263	F10014PC
A1U2	1820-1052	5	9	IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U3	1820-1173	1	11	IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A1U4	1820-0801	0	1	IC GATE ECL OR-NOR QUAD 2-INP	04713	MC10101P
A1U5	1810-0275	1	2	NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
A1U6	1810-0298	8	7	NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U7	1820-1399	3	1	IC FF ECL D-TYPE COM CLOCK HEX	04713	MC10176P
A1U8	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U10	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U11	1810-0275	1		NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
A1U12	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A1U13	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U14	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A1U15	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U16	1816-1462	2	1	IC ECL/10K 1024 (1K) STAT RAM 10-NS D-E	S0167	MBM10422H
A1U17	1810-0273	9	6	NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1U18	1816-1543	0	2	IC ECL/10K 4096 (4K) STAT RAM 25-NS D-E	28480	1816-1543
A1U19	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1U20	1816-1543	0		IC ECL/10K 4096 (4K) STAT RAM 25-NS D-E	28480	1816-1543
A1U21	1820-0826	9	1	IC GEN ECL PAR GEN 12-BIT	04713	MC10160L
A1U22	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1U23	1NB4-5009	0	1	COUNTER PKG.	28480	1NB4-5009
A1U24	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U25	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U26	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U27	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U28	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U29	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U30	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U31	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U32	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U33	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U34	1826-0856	7	1	IC CONV 8-B-D/A 20-DIP-P PKG	34335	AM6080APC
A1U35	1826-0544	0	1	V REF 8-DIP-C	04713	MC1403U
A1U36	1826-0271	0	1	IC OP AMP GP 8-DIP-P PKG	01295	SN72741P
A1U37	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A1U38	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A1U39	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A1U40	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A1U41	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1U42	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A1U43	1820-0804	3	1	IC GATE ECL NOR TPL	04713	MC10106P
A1U44	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1U45	1820-1475	6	5	IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U46	1820-1475	6		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U47	1820-1475	6		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U48	1820-1475	6		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U49	1820-1475	6		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U50	1820-1275	4	2	IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
A1U51	1816-0787	2	10	IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U52	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U53	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U54	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U55	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U56	1820-1491	6	1	IC BFR TTL LS NON-INV HEX 1-INP	01295	SN74LS367AN
A1U57	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A1U58	1820-0806	5	1	IC GATE ECL OR-NOR DUAL 4-5-INP	04713	MC10109P
A1U59	1820-2359	7		IC MISC ECL 14-INP	07263	F10014PC
A1U60	1816-1476	8	5	IC TTL 1024 (1K) STAT RAM 45-NS 3-S	28480	1816-1476
A1U61	1816-1476	8		IC TTL 1024 (1K) STAT RAM 45-NS 3-S	28480	1816-1476
A1U62	1816-1476	8		IC TTL 1024 (1K) STAT RAM 45-NS 3-S	28480	1816-1476
A1U63	1816-1476	8		IC TTL 1024 (1K) STAT RAM 45-NS 3-S	28480	1816-1476
A1U64	1816-1476	8		IC TTL 1024 (1K) STAT RAM 45-NS 3-S	28480	1816-1476
A1U65	1820-1275	4		IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
A1U66	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U67	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U68	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U69	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U70	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U71	1820-1730	6	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A1U72	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1U73	1820-0681	4	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A1U74	1820-0688	1	1	IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
A1U75	1820-1323	3	1	IC GATE TTL S NAND 8-INP	01295	SN74S30N
A1U76	1820-1997	7	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A1U77	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A1U78	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A1U79	1820-2550	0	1	IC DCDR TTL LS 3-TO-8-LINE	01295	SN74LS137N
A1U81	1820-1199	1	4	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A1U82	1820-1216	3	2	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A1U83	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A1U84	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A1U85	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1U86	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A1U87	1820-1430	3	5	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A1U88	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A1U89	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A1U90	1820-1282	3	2	IC FF TTL LS J-K BAR POS-EDGE-TRIG	01295	SN74LS109AN
A1U91	1820-1191	3	1	IC FF TTL S D-TYPE POS-EDGE-TRIG COM	01295	SN74S175N
A1U92	1816-1308	5	5	IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U93	1816-1308	5		IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U94	1816-1308	5		IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U95	1816-1308	5		IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U96	1816-1308	5		IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U97	1820-1282	3		IC FF TTL LS J-K BAR POS-EDGE-TRIG	01295	SN74LS109AN
A1U98	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A1U99	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A1U100	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A1U101	1820-1322	2	1	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
A1U102	1820-1782	8	1	IC MV TTL S MONOSTBL RETRIG/RESET DUAL	34335	AM26S02PC
A1U103	1820-1015	0	3	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
A1U104	1820-1015	0		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
A1U105	1820-1015	0		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
A1U106	1818-1596	7	4	IC CMOS 4096 (4K) STAT RAM 55-NS 3-S	S4013	HM6147P-3
A1U107	1818-1596	7		IC CMOS 4096 (4K) STAT RAM 55-NS 3-S	S4013	HM6147P-3
A1U108	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A1U109	1820-1428	9	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS158N
A1U110	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A1U111	1820-1428	9		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS158N
A1U112	1820-1858	9	1	IC FF TTL LS D-TYPE OCTL	01295	SN74LS377N
A1U113	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A1U114	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A1U115	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A1U116	1820-0269	4	1	IC GATE TTL NAND QUAD 2-INP	01295	SN7403N
A1U117	1820-2102	8	3	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
A1U118	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1U119	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
A1U120	1818-1596	7		IC CMOS 4096 (4K) STAT RAM 55-NS 3-S	S4013	HM6147P-3
A1U121	1818-1596	7		IC CMOS 4096 (4K) STAT RAM 55-NS 3-S	S4013	HM6147P-3
A1XU4	1200-0607	0	17	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU23	1200-0654	7	1	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A1XU25	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU27	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU29	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU31	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU33	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU36	1200-0796	8	1	SOCKET-IC 8-CONT DIP DIP-SLDR	28480	1200-0796
A1XU51	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU52	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU53	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU54	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU55	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU66	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU67	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU68	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU69	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU70	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU86	1200-0638	7	1	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A1XU92	1200-0612	7	5	SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU93	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU94	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU95	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU96	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU102	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
MP1	2200-0147	4	2	SCREW-MACH 4-40 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
MP2	2200-0151	0	2	SCREW-MACH 4-40 .75-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
MP3	64620-67601	7	1	HOOD-CONNECTOR ASSEMBLY (TOP)	28480	64620-67601
MP4	64620-67602	8	1	HOOD-CONNECTOR ASSEMBLY (BOTTOM)	28480	64620-67602
MP5	7121-2163	5	1	LABEL-DATA PROBE	28480	7121-2163
W2	64620-61601	5	1	CABLE-DATA ASSEMBLY	28480	64620-61601

Table 6-3. List of Manufacturers' Codes

Mfr No.	Manufacturer Name	Address		Zip Code
S0167	FUJITSU LTD	TOKYO	JP	
S4013	HITACHI	TOKYO	JP	
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
02111	SPECTROL ELECTRONICS CORP	CITY OF IND	CA	91745
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
11236	CTS OF BERNE INC	BERNE	IN	46711
19701	MEPCO/ELECTRA CORP	MINERAL WELLS	TX	76067
20932	EMCON DIV ITW	SAN DIEGO	CA	92129
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
25403	AMPEREX ELEK CORP SEMICON & MC DIV	SLATERSVILLE	RI	02876
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
27167	CORNING GLASS WORKS (WILMINGTON)	WILMINGTON	NC	28401
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
3L585	RCA CORP SOLID STATE DIV	SOMERVILLE	NJ	
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE	CA	94086
52763	STETTNER-TRUSH INC	CAZENOVIA	NY	13035
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
72136	ELECTRO MOTIVE CORP	FLORENCE	SC	06226
75042	TRW INC PHILADELPHIA DIV	PHILADELPHIA	PA	19108

SECTION VII

MANUAL BACKDATING

7-1. INTRODUCTION.

7-2. This section contains information required to backdate or update this manual for a specific repair number prefix.

7-3. MANUAL CHANGES.

7-4. This manual applies directly to the instrument having the repair number prefix shown on the manual title page. If the repair prefix is not the same as the one on the title page, find your repair number prefix in Table 7-1 and make the changes to the manual that are listed for that repair number prefix. When making changes listed in table 7-1, make the change with the highest number first. Example: if backdating changes 1,2 and 3 are required for your repair number, do change 3 first, then change 2, and finally change 1.

7-5. If the repair number of your instrument is not listed either on the title page or in table 7-1, refer to an enclosed MANUAL CHANGES sheet for updating information. Also, if a MANUAL CHANGES sheet is supplied, make all indicated ERRATA corrections.

Table 7-1. Manual Changes

PREFIX	MAKE CHANGES
2144	1
2250	1,2

CHANGE 1

Section VI

Page 20ACQ 6-4, Table 6-2. Replaceable Parts List,

Change A1 part number from 64623-66502 to 64623-66501. Check Digit from 8 to 7. Mfr Part Number from 64623-66502 to 64623-66501.

Page 20ACQ 6-5, Table 6-2. Replaceable Parts List,

Change A1U1 quantity from 2 to 1.

Page 20ACQ 6-6, Table 6-2. Replaceable Parts List,

Delete A1U59, 1820-2359, 7, -, IC MISC ECL 14-INP, 07263, F10014PC.

Section VIII

Schematics, Service Sheets 1 through 8,

Change the board number in the upper left corner from 64623-66502 to 64623-66501.

Page 20ACQ 8-19, Service Sheet 3,

Delete U59, Active Termination from J2 pins 7 and 11.

CHANGE 2

Section VI

Page 20ACQ 6-4, Table 6-2. Replaceable Parts List,

Change A1 Part Number from 64623-66503 to 64623-66502. Check Digit from 9 to 8. Mfr Part Number from 64623-66503 to 64623-66502.

Delete A1C57.

Change A1C1 quantity from 50 to 49.

Section VIII

Component Locators, Service Sheets 1 through 8,

Delete C57.

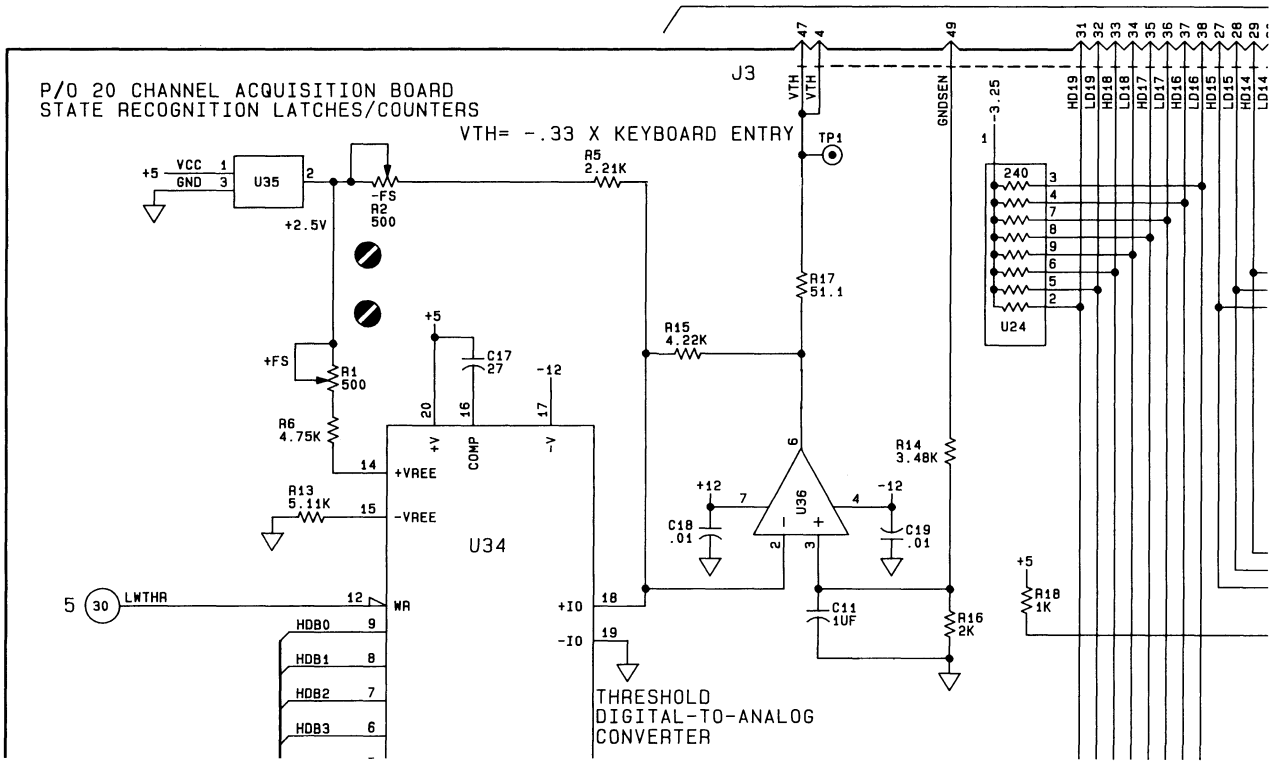
Schematics, Service Sheets 1 through 8,

Change the board number in the upper left corner from 64623-66503 to 64623-66502.

Page 20ACQ 8-15, Service Sheet 1,

Delete C57.

Move R17, 51.1 Ohm Resistor as shown below:



NOTES

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2. This section contains information for troubleshooting and repairing the Model 64623A 20 Channel State Acquisition Board.

8-3. The block diagram, schematic, component location figure, and other service information are provided on fold-out service sheets to help you in servicing the Model 64623A.

8-4. Normally, Theory of Operation is provided in this Section. However, the Model 64623A 20 Channel State Acquisition Board cannot function without a Model 64621A State Analysis Control Board, and for the purpose of the Theory of Operation, the two models are considered as one unit. Therefore, only limited Theory of Operation is provided in this manual. The Model 64621A State Analysis Control Board Service Manual, Section VIII, Service, provides more Theory of Operation at the State Analyzer Subsystem level.

8-5. Because the 20 Channel State Acquisition Board is very software dependent, it becomes very difficult to discuss the Theory of Operation at the bit level. Therefore, the following discussion is at the concept level of various functions.

8-6. 20 CHANNEL BLOCK DIAGRAM.

8-7. The Model 64623A 20 Channel State Data Acquisition Board consists of the following nine basic functional groups:

* State Recognition Latch/Counter and D/A Converter
* Resource Pattern Recognition
* Sequencer Pattern Recognition
* Trace Pod Data Memory
* Mainframe Interface
* Overview State/Time Counter
* Overview Event/Range Decode Memory
* Overview Event Pipeline Register
* Overview Event Memory

8-8. 20 CHANNEL BLOCK DIAGRAM THEORY.

8-9. STATE RECOGNITION LATCH/COUNTER.

* When in the latch mode, the State Recognition Latch, U45-U49, captures incoming data from the Data Probe.

* The information is latched using the clock strobe coming from the Control Board.

* When in the count (load) mode, the outputs of U45-U49 are used for stimulating the State Analyzer during Performance Verification.

* When the Mainframe is programming the State Analyzer, U45-U49 are used in the count mode to address the Resource Pattern Recognition, Sequence Pattern Recognition, and Overview Event/ Range Decode Memory.

* The D/A Converter sets the threshold for the Data Probe. It is controlled by the keyboard.

8-10. RESOURCE PATTERN RECOGNITION.

* The Resource Pattern Recognition circuitry is a group of Random Access Memories (RAMs) and 8 translators used to recognize patterns of data from the State Recognition Latch.

* The information to be analyzed is used to address the memories. When the address (information) is equal to the location at which ones were stored, those ones will appear at the outputs of the memories, thus indicating that the event has been recognized.

* The translators transmit the Resource Pattern to the Analysis Controller on the Control Board.

8-11. SEQUENCE PATTERN RECOGNITION.

* The Sequence Pattern Recognition circuitry is a group of RAMs and several gates used to recognize sequences of data from the State Recognition Latch.

* The Sequence State and the information to be analyzed is used to address the memories. When the address (information) is equal to the location at which ones were stored, those ones will appear at the outputs of the memories, thus indicating that the sequence pattern has been found.

* The outputs of the memories are sent to the Sequencer on the Control Board.

8-12. TRACE POD DATA MEMORY.

* The Trace Pod Data Memory consists of RAMs, latches (Pipeline Register) and data selectors for chip selection, and address counters.

* The Pipeline Register, U76-U78, holds information until the memories are ready to accept the information to be stored.

* The memories, U92-U96, store 256 words of the information being analyzed, to be formatted by the Mainframe CPU and displayed on the CRT at a later time.

* The data selectors provide the addresses for the memories. In the write mode, the addresses come from the Address Counters, U108 and U110. In the read mode, the addresses are provided by the Mainframe CPU.

8-13. MAINFRAME INTERFACE.

* The Mainframe Interface consists of various latches and buffers for interfacing the State Analyzer's circuits to the Mainframe.

* Through the use of read and write decoders, the Mainframe can select various groups of circuitry on the Acquisition Board and write to (program) or read from (verify, interrogate) them over the Mainframes Data Bus.

8-14. OVERVIEW STATE/TIME COUNTER.

* A major part of the Overview State/Time Counter is the LSI Counter, U23, a 20 bit floating point gray code counter referenced to a 25 MHz crystal located in the Mainframe.

* The State/Time Counter is reset and allowed to count the number of states or time for each interval to be measured. When the interval being measured begins, the Counter is reset. When the interval ends, the output value of the counter is compared to one of fifteen values or ranges requested by the operator using the Overview Event/Range Decode Memory. If the value is the same as or is within the range defined, that event number is stored in the Overview Event Memory. If the value is not within the range defined, then a false status is stored.

8-15. OVERVIEW EVENT/RANGE DECODE MEMORY.

* The Overview Event/Range Decode Memory in general is three RAMs, U16, U18 and U20. The RAMs are used to determine if the output value of the Overview State/Time Counter or the user's information from U37 -41 falls into one of as many as 15 events or one of up to four ranges. If the value is not one of the 15 events defined by the operator of the system (keyboard entry), then it falls into the sixteenth category called the null event.

* The code generated by the Overview Event/Range Decode Memory is unique and is stored in the Overview Event Pipeline Register temporarily, then stored in the Overview Event Memory.

* Later the Mainframe CPU will read the code stored, and count the number of times each event occurred, building a histogram, graph, or list on the CRT.

* When the State Analyzer is not using Overview, this memory can send up to four range patterns to the Control Board to be used to qualify triggering, storage, or count.

8-16. OVERVIEW EVENT PIPELINE REGISTER.

* The Overview Event Pipeline Register is a four bit latch, U91, that latches the code output of the Overview Event/Range Decode Memory. The code is then presented to the Overview Event Memory for storage.

8-17. OVERVIEW EVENT MEMORY.

* The Overview Event Memory, U106, U107, U120, and U121 is used to store the code generated by the Overview Event/Range Decode Memory.

* Data selectors, U103 -105, provide the address for the memory. During the write mode the address comes from the Overview Memory Address Counters, U87-U89. In the read mode, the address comes from the Mainframe CPU.

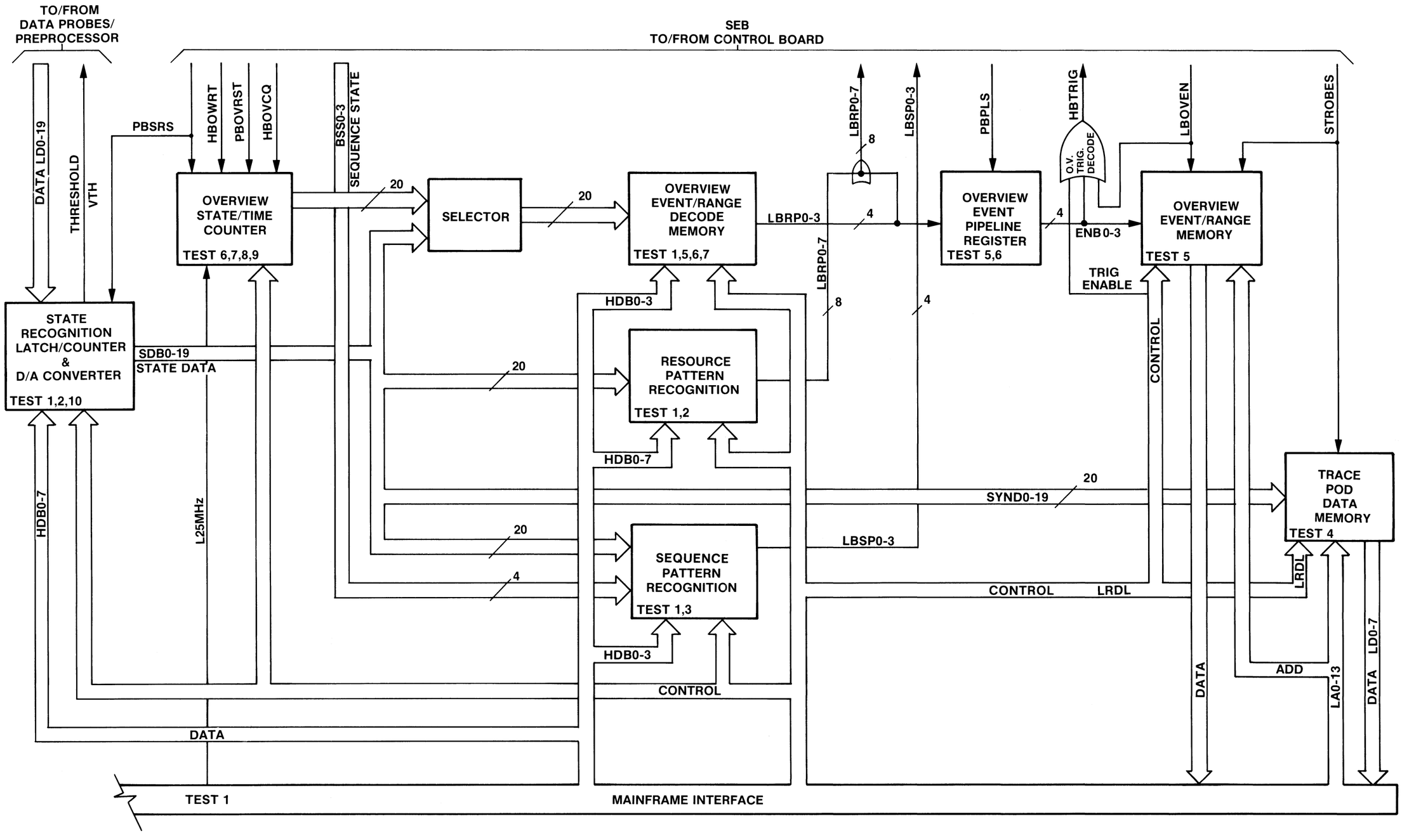


Figure 8-1.
20 Channel ACQ Block Diagram
20ACQ 8-4

8-18. MNEMONICS.

8-19. The signals in this product have been assigned mnemonics that indicate the true state, and the function of the signal line. In general the first character indicates the true state, H for high, l for low. If the signal is used with an edge sensitive device, P for positive, and N for negative is used to indicate the edge that the signal becomes true on. No indication of the voltage levels is given, i.e., TTL, ECL, MOS. This information is given on the schematic using the newer type of Logic Symbology.

Table 8-1. Mnemonics

Mnemonic	Description
BSS0-3	Bus Sequence State 0-3 -- a feedback path within the Control Board Sequencer that enables it to change from one state to the next. A state may require that an event occur only once, or it may require the event to occur many times before changing to the next state. BSS0-3 develops SSB0-3.
CNT0-19	Count 0-19 -- outputs of the Overview State/Time Counter. CNT0-19 are wire ORed with HRNG0-19. HRNGSEL selects which one is active. CNT0-19 is used to count the number of states or amount of time between states when in the Overview mode. See HRNG0-19.
GNDSEN	Ground Sense -- the return path from the Data Probe for the Data Threshold Digital to Analog Converters.
HAB0-2	High Address Buffered 0-2 -- same as the CPU Address Bus (LA0-13) except inverted. HAB0-2 is used to develop select lines for the Trace Pod Data Memories (LTMS0-4).
HBOTF	High Bus Overview Trigger Flag --sent to the Control Board. When high, indicates that the 20 Channel Acquisition Board has seen a qualified overview trigger event. (A trigger event is a single occurrence of an event decoded from input data or from the Overview State/Time Counter.)
HBOVCQ	High Bus Overview Count Qualify -- from the Control Board. When high, HBOVCQ allows the Overview Counter to increment. HBOVCQ is driven by the Analysis Controller or HOVCQ on the Control Board.
HBOWRT	High Bus Overview Write -- a write strobe from the Control Board. When enabled on the 20 Channel Data Acquisition Board, HBOWRT allows the Overview Event Memories to be written to, and increments the Overview Memory Address Counters.
HBQWRT	High Bus Qualified Write -- when high, HBQWRT synchronizes data storage in the Trace Pod Data Memories on the Acquisition Boards with the Trace Counter/Status Memories on the Control Board. When low, HBQWRT increments the Trace Pod Data Memory Address Counters on the Data Acquisition Boards. HBQWRT is enabled by HWQ, and is derived from HWRT on the Control Board.
HCLRCNT	High Clear Counter -- a signal generated by the CPU. When high, HCLRCNT resets the State Recognition Latch/Counters for the Data Pod.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
HCTST	High Count Test -- used when testing the Overview State/Time Counter. When high, HCTST divides the Counter into two ten bit counters. HCTST is controlled by the CPU.
HD0-19	High Data 0-19 -- differential data signals (LD0-19) generated by the equipment being monitored. HD0-19 may come from either the Data Probes or the Preprocessor.
HDATAV	High Data Valid -- a status signal returned to the CPU. When high, HDATAV indicates the point in time that the CPU can read from the Overview Event Memories.
HDB0-7	High Data Buffered 0-7 -- same as the CPU Data Bus (LD0-7) except inverted. HDB0-7 is the path the CPU uses when it wants to input data to various circuits on the Data Acquisition Board.
HMA0-7	High Memory Address 0-7 -- developed by the Trace Pod Data Memory Address Counters or the CPU (LA4-11) on the Data Acquisition Board. Used to address the Trace Pod Data Memories.
HMCEN	High Measurement Complete Enable -- developed by the CPU in the Counter Latch. When high, HMCEN allows the terminal count of the Overview Memory Address Counter to be latched into the Measurement Complete Detector. This causes LMCOMP to go low.
HNEVEN	High Null Event -- a CPU controlled signal. When high, HNEVEN enables the Null Event Decoder, which in turn enables storage of null events in the Overview Event Memory. When low, HNEVEN excludes the storage of null events in the Overview Event Memory.
HOMA0-11	High Overview Memory Address 0-11 -- HOMA0-11 is used to address the Overview Event Memories. HOMA0-11 is generated by either the Overview Memory Address Counter (LOMC0-11) or the CPU (LA0-11).
HOTEN	High Overview Trigger Enable -- developed by the CPU. HOTEN becomes LOTEN. When high, HOTEN enables the Overview Trigger Decode Circuit. The Overview Trigger Decode produces HBOTF from outputs of the Overview Event/Range Decode Memories, LBOVEN, and LOTEN (see HBOTF).
HOVEQ	High Overview Enable Qualifier -- derived from LBOVEN. When high, HOVEQ qualifies write cycles to the Overview Event Memories.
HRNG0-19	High Range 0-19 -- developed from the equipment being monitored (SYND0-19). HRNG0-19 is input to the Overview Event/Range Decode Memories. The outputs of the Memories indicate if the monitored information is within the range specified from the keyboard. See CNT0-19.
HRNGSEL	High Range Select -- a CPU controlled signal that selects ranging on input data or counter data. When high, HRNGSEL enables the Pod Data TTL-ECL Translators. The outputs of the Translators are wire ORed with the outputs

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
	of the Overview State/Time Counter. When low, HRNGSEL enables the outputs of the Counter.
HRP0-7	High Resource Pattern 0-7 -- outputs of the Resource Pattern Memories. When high, HRP0-7 indicates that combinations of Trigger, Storage, and Count information have been detected. HRP0-7 becomes LBRP0-7 and is sent to the Control Board.
HSTM	High Start Memory -- a signal originating in the Mainframe. When high, HSTM indicates that the information on the CPU's Address Bus is valid.
HWRAP	High Wrap -- a status signal returned to the CPU. When high, HWRAP indicates that the Overview Event Memories are full of information.
L25MHZ	Low 25 Megahertz -- a high accuracy crystal controlled clock originating in the Mainframe. L25MHZ is used to clock the Overview State/Time Counter when in the time mode for measuring time between states.
LA0-13	Low Address 0-13 -- a 16 bit address bus used by the CPU to address various devices in the system. The Address Bus is transmit only from the CPU. Only bits 0-13 are used in this model.
LBCLR	Low Bus Clear -- LBCLR comes from the Control Board. When low, LBCLR resets the Trace Pod Data Memory Address Counter and the Overview Memory Address Counter.
LBMACS	Low Bus Memory Address Counter Select -- developed in the Control Board Strobe Generator. In the 20 Channel Data Acquisition Board, LBMACS allows the Memory Address Counters to address the Trace Pod Data Memories when low. When high, the CPU can address the Memories over the CPU Address Bus. When low, LBMACS also allows the Overview Memory Address Counter to address the Overview Event Memories.
LBOVEN	Low Bus Overview Enable -- from the Control Board. When low, LBOVEN allows the Overview section to look for its Trigger Events (see HBOTF). LBOVEN produces HOVEQ.
LBRP0-7	Low Bus Resource Pattern 0-7 -- eight signals going to the Control Board. When low, indicates to the Analysis Controller that combinations of Trigger, Storage, and Count information have been detected.
LBSP0-3	Low Bus Sequence Pattern 0-3 -- four signals going to the Control Board. When low, they indicate to the Sequencer that the Data Acquisition Boards have found the Sequence State(s) requested by the user.
LD0-15	Low Data 0-15 -- a 16 bit bidirectional bus used to transfer data to and from the CPU. When LSTB is low, the data on the bus is valid.
LD0-19	Low Data 0-19 -- differential data signals (HD0-19) from the user's equipment. LD0-19 may come from either the Data Probes or the Preprocessor.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
LED0-3	Low Event Data 0-3 -- outputs of the Event Data Holding Register that have been latched by HBOWRT (see LEV0-3).
LEV0-3	Low Event 0-3 -- outputs of the Overview Event/Range Decode Memory that represent user overview events.
LID	Low Identification -- a signal originating in the Mainframe. When low, the CPU is requesting that the Board Identification be sent from the State Analyzer Data Acquisition Board to the CPU over the Data Bus on data bits 10 and 12.
LLOAD	Low Load -- a signal generated by the CPU in the Control Latch. When low, the State Recognition Latch/Counters are in the count mode.
LMACS	Low Memory Address Counter Select -- developed in the Control Board Strobe Generator. When low, LMACS allows the Memory Address Counter to address the Trace Pod Data Memories. When high, the CPU can address the Memories over the CPU Address Bus.
LMAP2	Low Map 2 --a signal developed by the CPU. LMAP2 is used as the Start/Stop Pulse in Signature Analysis.
LMCOMP	Low Measurement Complete -- the output of the Measurement Complete Detector. When low, LMCOMP stops the Overview Memory Address Counter and stops the writing process to the Overview Event Memories. LMCOMP is also returned to the CPU through the Overview Memory Address Counter Latch.
LOCS	Low Overview Count Select -- when low, LOCS allows the Overview Memory Address Counter to address the Overview Event Memories (LOMC0-11 and HOMA0-11). When high, the CPU can address the Memories (LA0-11 and HOMA0-11).
LOMC0-11	Low Overview Memory Count 0-11 -- outputs of the Overview Memory Address Counter. LOMC0-11 is used to address the Overview Event Memories.
LOTEN	Low Overview Trigger -- developed by the CPU in the Control Latch. LOTEN is the same as HOTEN except inverted. When low, LOTEN enables the Overview Trigger Decode Circuit. The Overview Trigger Decode produces HBOTF from the outputs of the Overview Event/Range Decode Memories, LBOVEN, and LOTEN (see HBOTF).
LOVE0-3	Low Overview Event 0-3 -- outputs of the Overview Event Memory. LOVE0-3 are returned to the CPU through the Overview Event Data Latch.
LOWEN	Low Overview Write Enable -- developed from HNEVEN, HNEV0-3, and LWRAP. LOWEN enables the read/write line (LWOV) for the Overview Event Memories.
LPOP	Low Power On Preset -- when low (during Mainframe power-up or during A.C. power line disturbances), LPOP resets various latches, counters, and registers to a known state. When LPOP returns to a high state, the Mainframe begins executing software.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
LQWS	Low Qualified Write Strobe -- same as HBQWRT except inverted. LQWS when low, allows data to be written to the Trace Pod Data Memories. When going from a low state to a high state, LQWS increments the Trace Pod Data Memory Address Counters.
LRANGE	Low Range -- developed by the CPU in the Control Latch. When low, LRANGE enables the Range Buffers. When the Range Buffers are enabled, output information from the Overview Event/Range Decode Memories is wire ORed with LBRP0-3 (Resource Patterns).
LRDL	Low Read Data Latch -- developed by the CPU in the Mainframe Interface. The CPU forces LRDL low when it wants to read the information in the Trace Pod Data Latch (LD0-7) and the Overview Event Data Latch (LD8-15).
LRDOV	Low Read Overview -- developed by the CPU in the Mainframe Interface. The CPU forces LRDOV low when it wants to read the information in the Overview Memory Address Counter Latch (LD0-15).
LSEL	Low Select -- a signal originating in the Mainframe. When low, LSEL allows the State Analyzer Identification Code to be returned over the CPU's Data Bus. This allows the CPU to identify if there is a State Analyzer Data Acquisition Board installed in the Mainframe, and if so which slot of the Card Cage it is installed in. LSEL is also used to enable the State Analyzer Data Acquisition Board.
LSEQ0-19	Low Sequence 0-19 -- outputs of the Sequence Pattern Memories. When decoded, LSEQ0-19 produce LBSP0-3.
LSTATE	Low State -- LSTATE controls the two modes of the Overview State/Time Counter. When LSTATE is low, the Counter counts the number of states between two stored states. PINC is used to increment the Counter in the state mode. When LSTATE is high, the Counter counts time using L25MHZ as a reference.
LSTB	Low Strobe -- a signal originating in the Mainframe. When low and the CPU is in the write mode (LWRT low), LSTB indicates the Data Bus has valid information on it. When low and in the read mode, LSTB indicates that the CPU is not driving the Data Bus, and the device addressed may now drive it.
LSTM	Low Start Memory -- a signal originating in the Mainframe. When low, LSTM indicates that the information on the CPU's Address Bus is valid.
LTMS0-4	Low Trace Memory Select 0-4 -- developed by the CPU Address Bus in the RAM Selector. LTMS0-4 selects one of five Trace Pod Data Memories. The output of the selected Memory is latched into the Trace Pod Data Latch.
LWDM1-3	Low Write Decoder Memories 1-3 -- developed by the CPU in the Write Decoders. LWDM1-3 controls the read and write modes of the Overview Event/Range Decode Memories. When LWDM is low, the Memory is in the write mode.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
LWOV	Low Write Overview -- developed from LOWEN and HBOWRT. LWOV is used to control the read/write mode of the Overview Event Memories. When LWOV is low, the Memories are in the write mode.
LWR0-4	Low Write Resource 0-4 -- developed by the CPU in the Write Decoders. When low, LWR0-4 allows the CPU to write information into the Resource Pattern Memories (HDB0-7).
LWRT	Low Write -- one of the control lines from the Mainframe. When low, the CPU is writing to the addressed device, i.e., the State Analyzer Data Acquisition Board.
LWS0-4	Low Write Sequence 0-4 -- developed by the CPU in the Write Decoders. When low, LWS0-4 allows the CPU to write information into the Sequence Pattern Memories (LDB0-7).
LWTHR	Low Write Threshold -- when LWTHR goes from a high state to a low state, information from the CPU is latched into the Digital to Analog Converter. The output current is proportional to the binary value latched. ((Full Scale Current X Binary Value Latched)/256 = Output Current.)
NBDSTB	Negative Bus Data Strobe -- a differential signal (PBDSTB), developed in the Control Board Strobe Generator. Used to latch the outputs of the Trace Pod Data Memories into the Trace Pod Data Latch on the Data Acquisition Boards.
NBSRS	Negative Bus State Recognition Strobe -- a differential strobe (PBSRS) developed in the Control Board Strobe Generator, and sent to the Data Acquisition Boards. At the begining of a data acquisition cycle, NBSRS goes from a high state to a low state. NBSRS is used to latch user information into the State Recognition Latch/Counters.
PBDSTB	Positive Bus Data Strobe -- a differential signal (NBDSTB), developed in the Control Board Strobe Generator. PBDSTB is used to latch the outputs of the Trace Pod Data Memories into the Trace Pod Data Latch on the Data Acquisition Boards.
PBOVRST	Positive Bus Overview Reset -- from the Control Board. When PBOVRST goes from a low state to a high state, the Overview State/Time Counter is reset.
PBPLS	Positive Bus Pipeline Strobe - used in the 20 Channel Data Acquisition Board for latching user information into Trace Pod Data Pipeline Registers at the correct time in the Analyzer's timing cycle.
PBRSTB	Positive Bus Read Strobe -- developed by the Control Board Strobe Generator. When PBRSTB goes from a low to a high state, the read address for the Trace Pod Data Memories is latched into the Memory Address Latch. When going from a high state to a low state, PBRSTB latches the Trace Pod Data Memory select line (LTMS0-4) into the RAM Selector.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
PBSRS	Positive Bus State Recognition Strobe -- a differential strobe (NBSRS) developed in the Control Board Strobe Generator, and sent to the Data Acquisition Boards. At the begining of a data acquisition cycle, PBSRS goes from a low state to a high state. PBSRS is used to latch user information into the State Recognition Latch/Counters.
PBSTBRQ	Positive Bus Strobe Request -- a signal going to the Control Board during Performance Verification only. When going from a low to a high state, PBSTRG begins a strobe generator cycle. PBSTBRQ is wire ORed with PPVSTB and HMCLK on the Control Board.
PINC	Positive Increment -- developed by the CPU. A path that can be used to increment the Overview State/Time Counter without a Strobe Generator cycle occuring.
PPLSTB	Positive Pipeline Strobe Buffered -- same as PBPLS except buffered. PPLSTB latches target system information into the Trace Pod Data Pipeline Registers at the correct time in the Analyzer's timing cycle.
PWCTL	Positive Write Control Latch -- developed by the CPU in the Write Decoders. PWCTL is used to clock HDB0-7 into the Control Latch. Eight control lines are developed in the Control Latch.
SD0-3	State Data 0-3 -- a four bit path from the Trace Pod Data Memories to the Trace Pod Data Latch. The CPU uses this path along with the CPU Data Bus to read information out of the Trace Pod Data Memories.
SSB0-3	Sequence State Buffered 0-3 -- same a BSS0-3 except buffered. BSS0-3 are developed by the Control Board Sequencer and enables it to change from one state to the next. A state may require that an event occur only once, or it may require the event to occur many times before changing to the next state.
SYND0-19	Synchronous Data 1-19 -- a data path from the State Recognition Latch/Counters to the Resource Pattern Memories, the Sequence Pattern Memories, and the Trace Pod Data Pipeline Registers.
SYNPD0-19	Synchronous Pipelined Data 0-19 -- a data path from the Trace Pod Data Pipeline Register to the Trace Pod Data Memories.
VTH	Voltage, Threshold -- a user programmable voltage sent to the Data Probe as a reference voltage for the Comparators.

Table 8-2. Schematic Diagram Notes

ETCHED CIRCUIT BOARD

FRONT PANEL MARKING

REAR-PANEL MARKING

MANUAL CONTROL

SCREWDRIVER ADJUSTMENT

TP1 ELECTRICAL TEST POINT TP (WITH NUMBER)

NUMBERED WAVEFORM NUMBER CORRESPONDS TO ELECTRICAL TEST POINT NO.

LETTERED TEST POINT NO MEASUREMENT AID PROVIDED

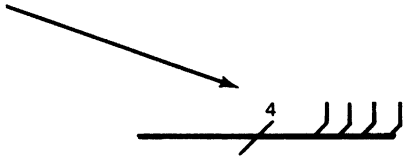
COMMON CONNECTIONS. ALL LIKE-DESIGNATED POINTS ARE CONNECTED.

1 3 NUMBER ON WHITE BACKGROUND = OFF-PAGE CONNECTION. LARGE NUMBER ADJACENT = SERVICE SHEET NUMBER FOR OFF-PAGE CONNECTION.

A CIRCLED LETTER = OFF-PAGE CONNECTION BETWEEN PAGES OF SAME SERVICE SHEET.

INDICATES SINGLE SIGNAL LINE

NUMBER OF LINES ON A BUS



(925) WIRE COLORS ARE GIVEN BY NUMBERS IN PARENTHESES USING THE RESISTOR COLOR CODE

[(925) IS WHT-RED-GRN]

0 - BLACK	5 - GREEN
1 - BROWN	6 - BLUE
2 - RED	7 - VIOLET
3 - ORANGE	8 - GRAY
4 - YELLOW	9 - WHITE

* OPTIMUM VALUE SELECTED AT FACTORY, TYPICAL VALUE SHOWN; PART MAY HAVE BEEN OMITTED.

UNLESS OTHERWISE INDICATED:
RESISTANCE IN OHMS
CAPACITANCE IN PICOFARADS
INDUCTANCE IN MICROHENRIES

μP	=	MICROPROCESSOR
P/O	=	PART OF
NC	=	NO CONNECTION
CW	=	CLOCKWISE END OF VARIABLE RESISTOR

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Table 8-3. Logic Symbology

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term.)

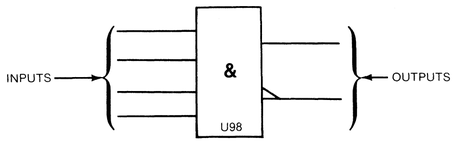
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

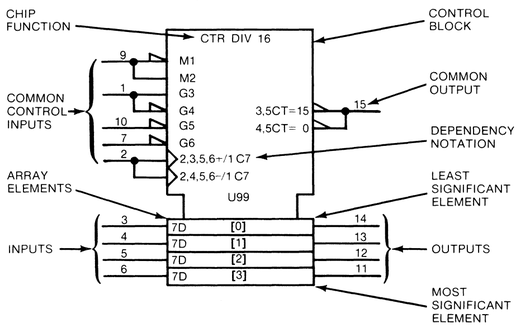
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. Unless indicated, the least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in **[ ]**).

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Table 8-3. Logic Symbology (Cont'd)

INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.

b. Interconnection (Z) indicates connections inside the symbol.

c. Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.

d. Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.

e. Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).

f. Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.

g. Address (A) identifies the address inputs.

h. Transmission (X) identifies bi-directional inputs and outputs that are connected together when the transmission input is true.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (complements state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection
		X	Transmission

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Table 8-3. Logic Symbology (Cont'd)

OTHER SYMBOLS

- Analog Signal
- & AND
- Bit Grouping
- Buffer
- ! Compare
- Dynamic
- =1 Exclusive OR
- Hysteresis
- ? Interrogation
- Internal Connection
- Inversion
- O Negation
- Nonlogic Input/Output
- Open Circuit (external resistor)
- Open Circuit (external resistor)
- ≥1 OR
- Passive Pull Down (internal resistor)
- Passive Pull Up (internal resistor)
- Postponed
- ← Shift Left (or up)
- → Shift Right (or down)
- / Solidus (allows an input or output to have more than one function)
- ▽ Three State
- , Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.
- ( ) Used for factoring terms using algebraic techniques.
- [ ] Information not defined.
- Φ Logic symbol not defined due to complexity.

LABELS

BG	Borrow Generate	CO	Carry Output	J	J Input
BI	Borrow Input	CP	Carry Propagate	K	K Input
BO	Borrow Output	CT	Content	P	Operand
BP	Borrow Propagate	D	Data Input	T	Transition
CG	Carry Generate	E	Extension (input or output)	+	Count Up
CI	Carry Input	F	Function	-	Count Down

MATH FUNCTIONS

Σ	Adder	>	Greater Than
ALU	Arithmetic Logic Unit	<	Less Than
COMP	Comparator	CPG	Look Ahead Carry Generator
DIV	Divide By	π	Multiplier
=	Equal To	P-Q	Subtractor

CHIP FUNCTIONS

BCD	Binary Coded Decimal	DIR	Directional	RAM	Random Access Memory
BIN	Binary	DMUX	Demultiplexer	RCVR	Line Receiver
BUF	Buffer	FF	Flip-Flop	ROM	Read Only Memory
CTR	Counter	MUX	Multiplexer	SEG	Segment
DEC	Decimal	OCT	Octal	SRG	Shift Register

DELAY and MULTIVIBRATORS

- Astable
- Delay
- Nonretriggerable Monostable
- NV Nonvolatile
- I State of initial power up
- Retriggerable Monostable

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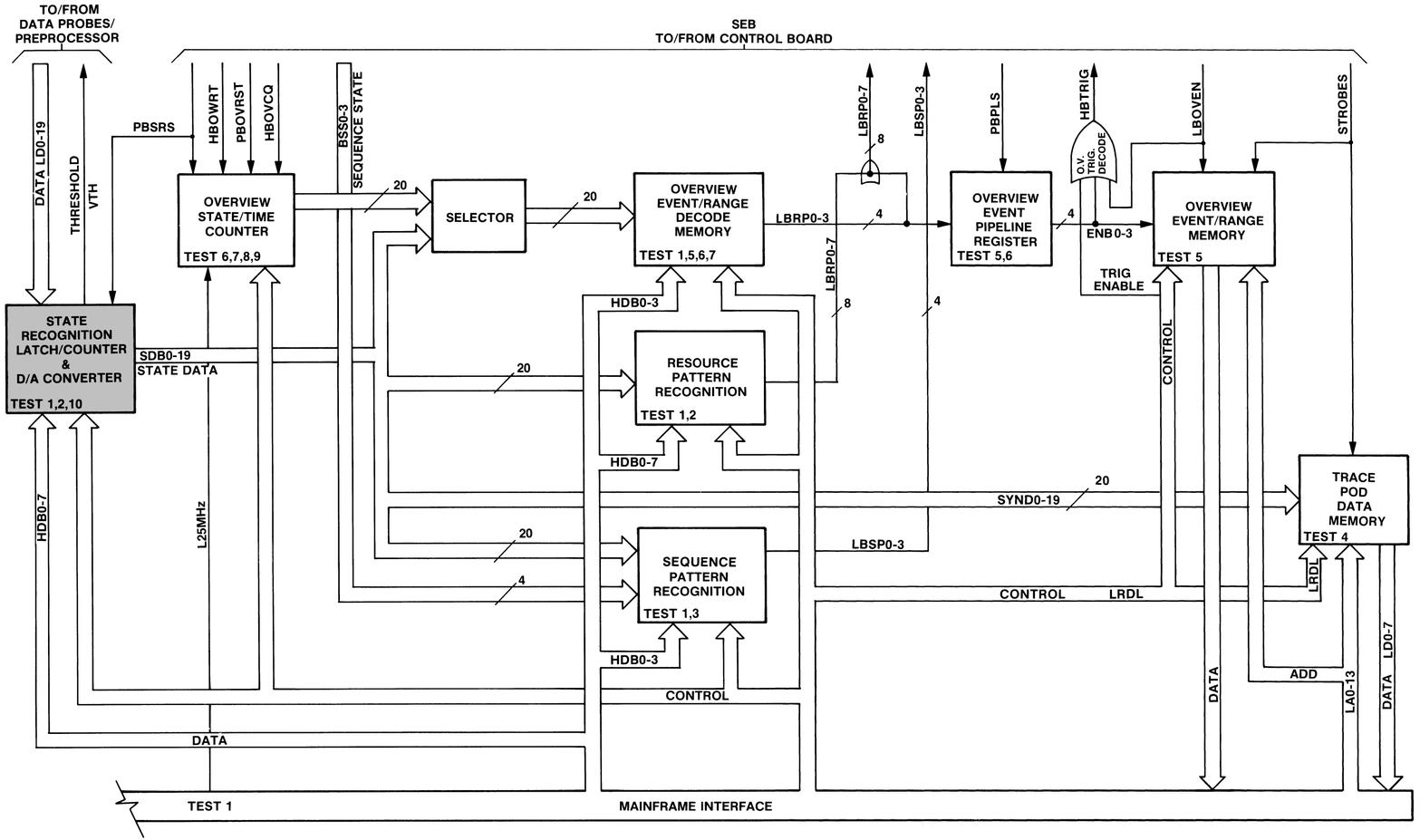
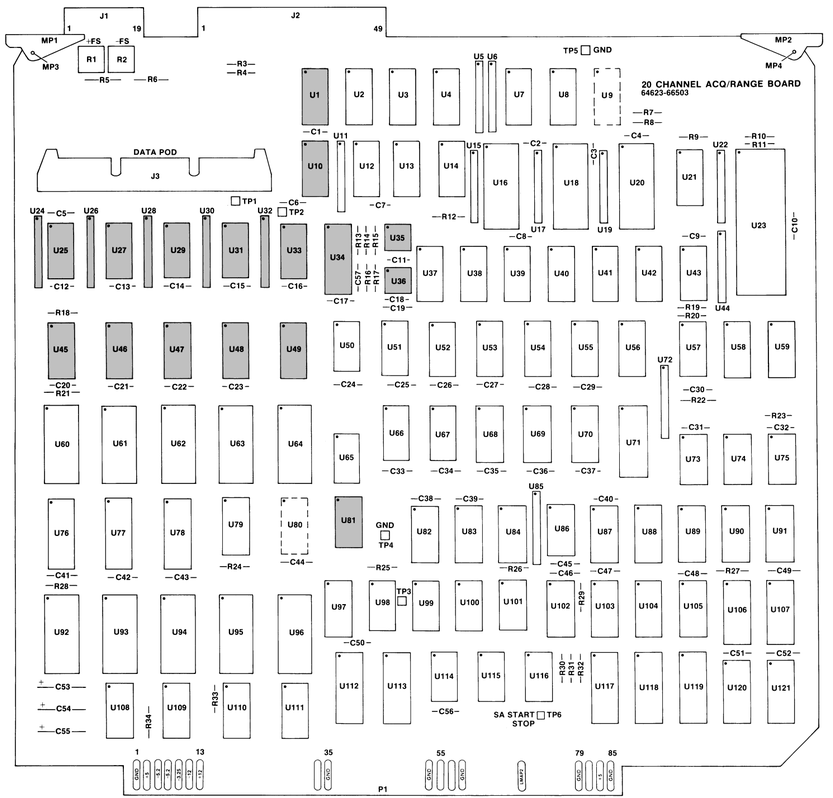
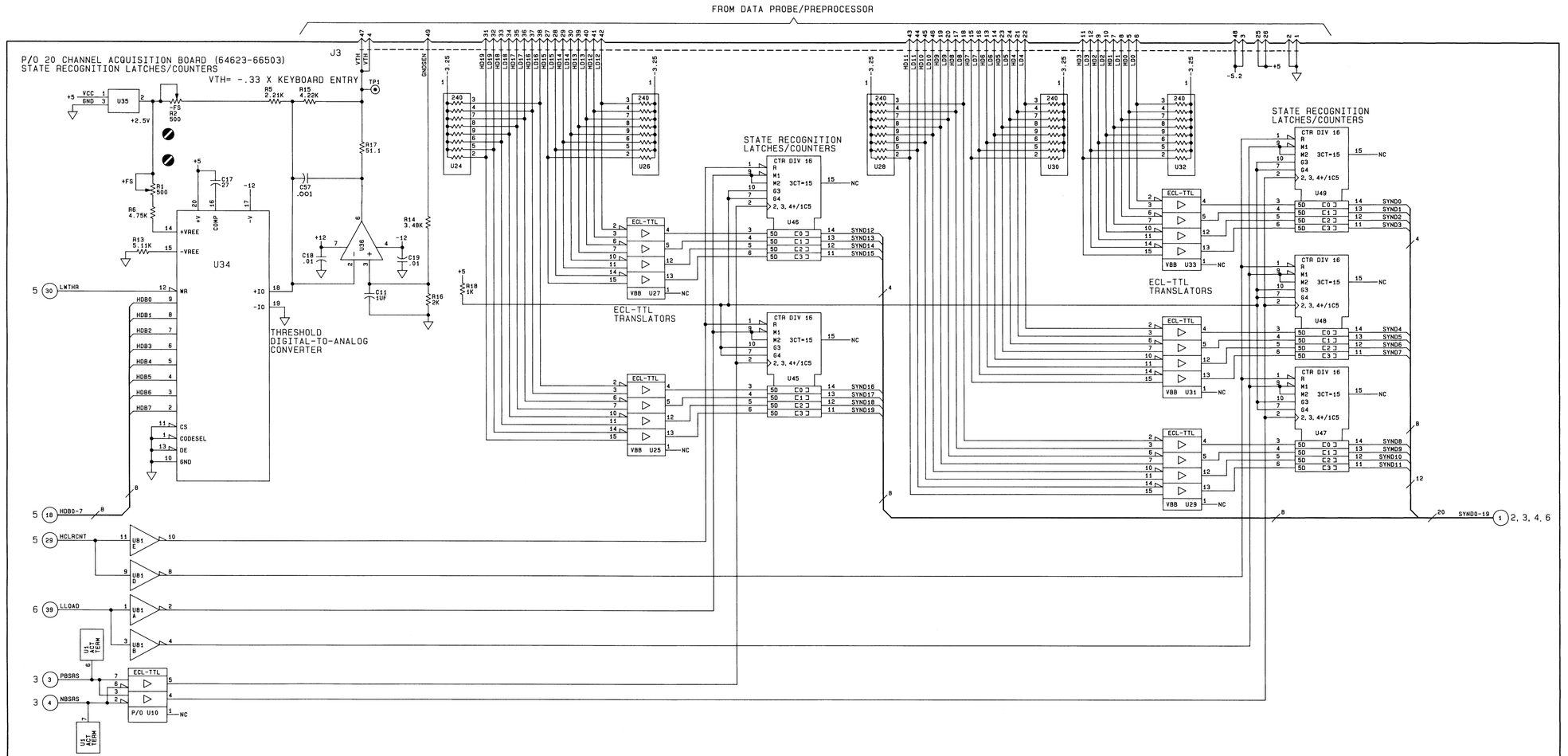


Block Diagram



Component Locator



ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG PART NO.
U10,25,27, 29,31,33	1820-1052	MC10125L
U45-49	1820-1475	93S16DC
U81	1820-1199	SN74LS04N

PARTS ON THIS SCHEMATIC

C11,17,18,19
J3
R1,2,5,6,13-17
TP1
U1,10,24-36,45-49,81

IC POWER SUPPLY CONFIGURATIONS

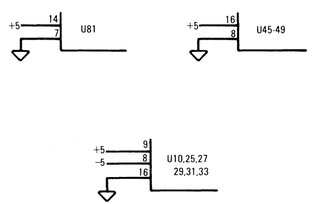
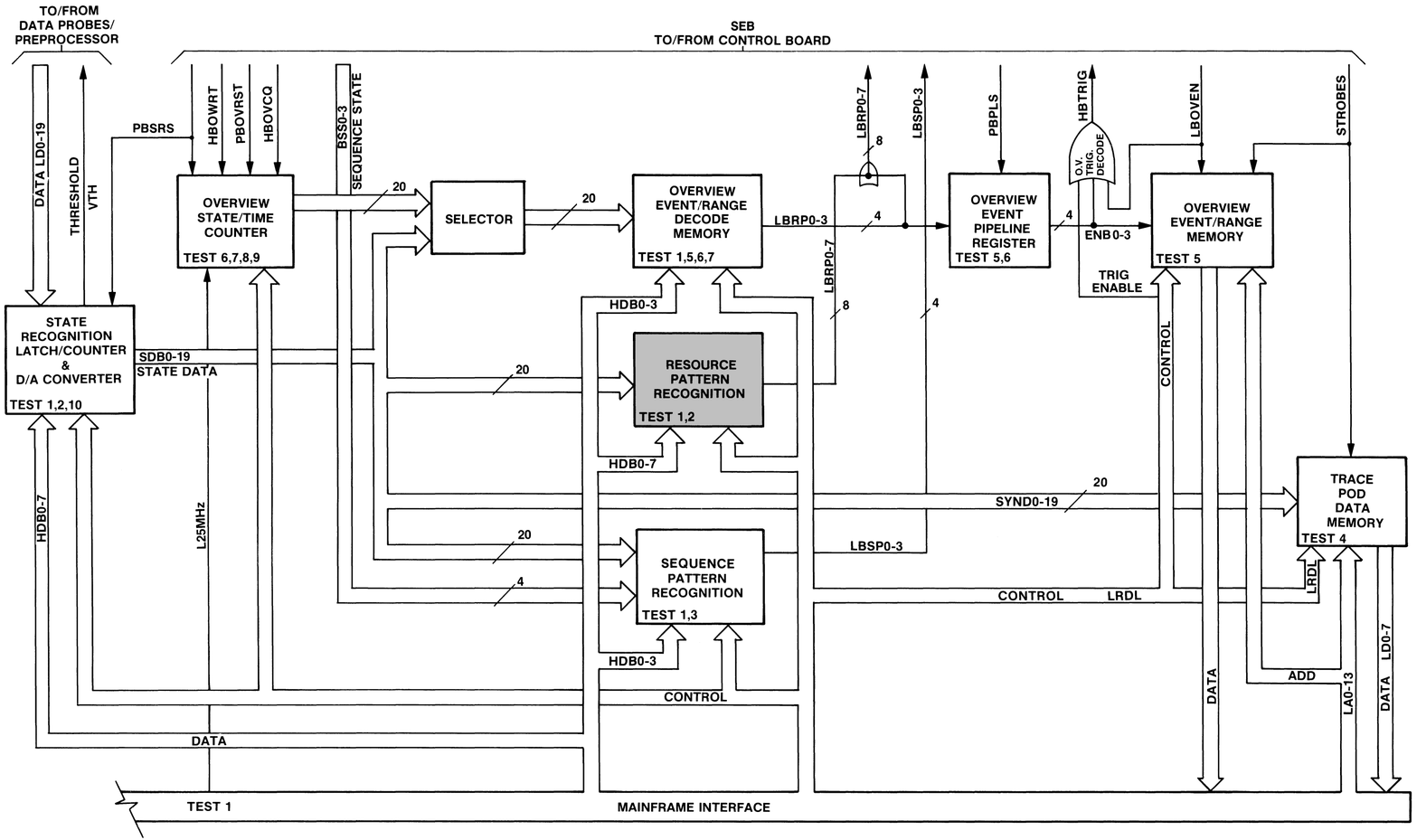
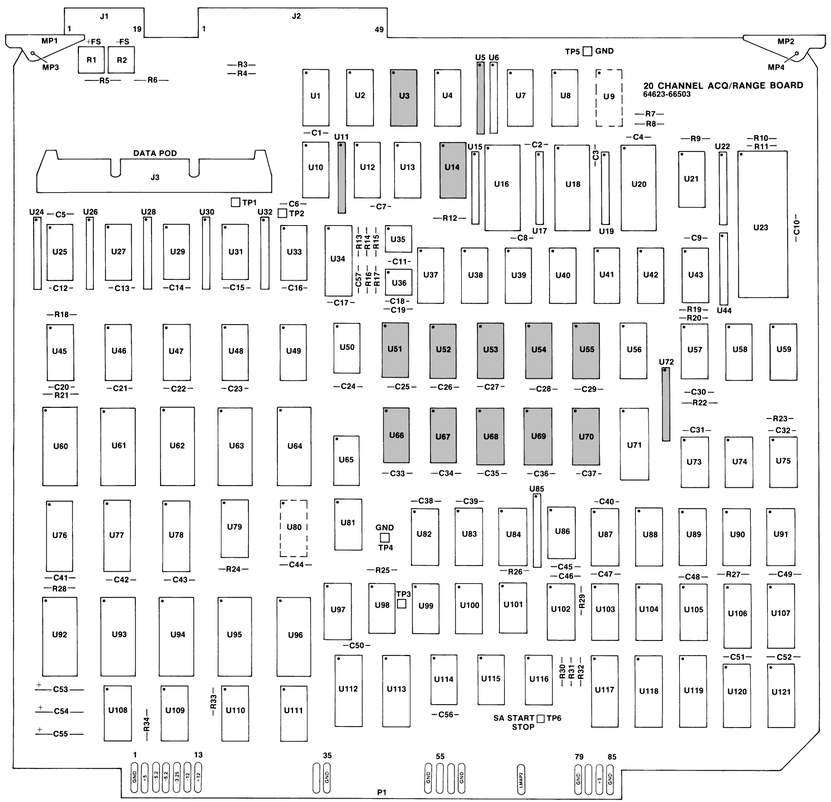


Figure 8-2.
State Recognition Latch/Counter
20ACQ 8-15



Block Diagram



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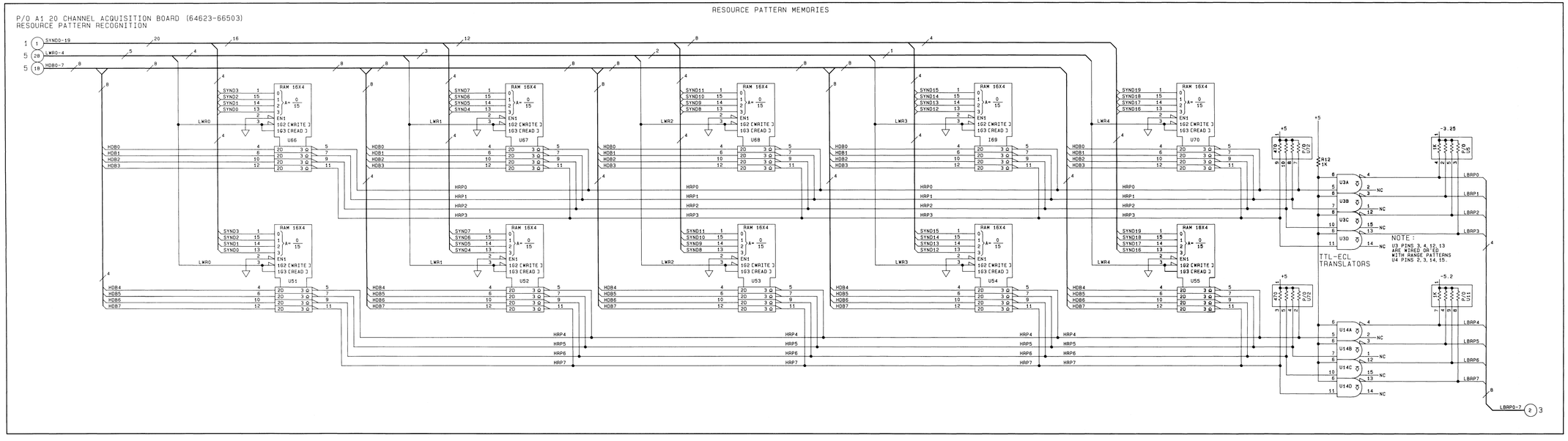


ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG PART NO.
U3,14	1820-1173	MC10124L
U51-55,66-70	1816-0787	SN74S289N

PARTS ON THIS SCHEMATIC

R12 U3,5,11,14,51-55,66-70,72

IC POWER SUPPLY CONFIGURATIONS

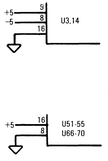
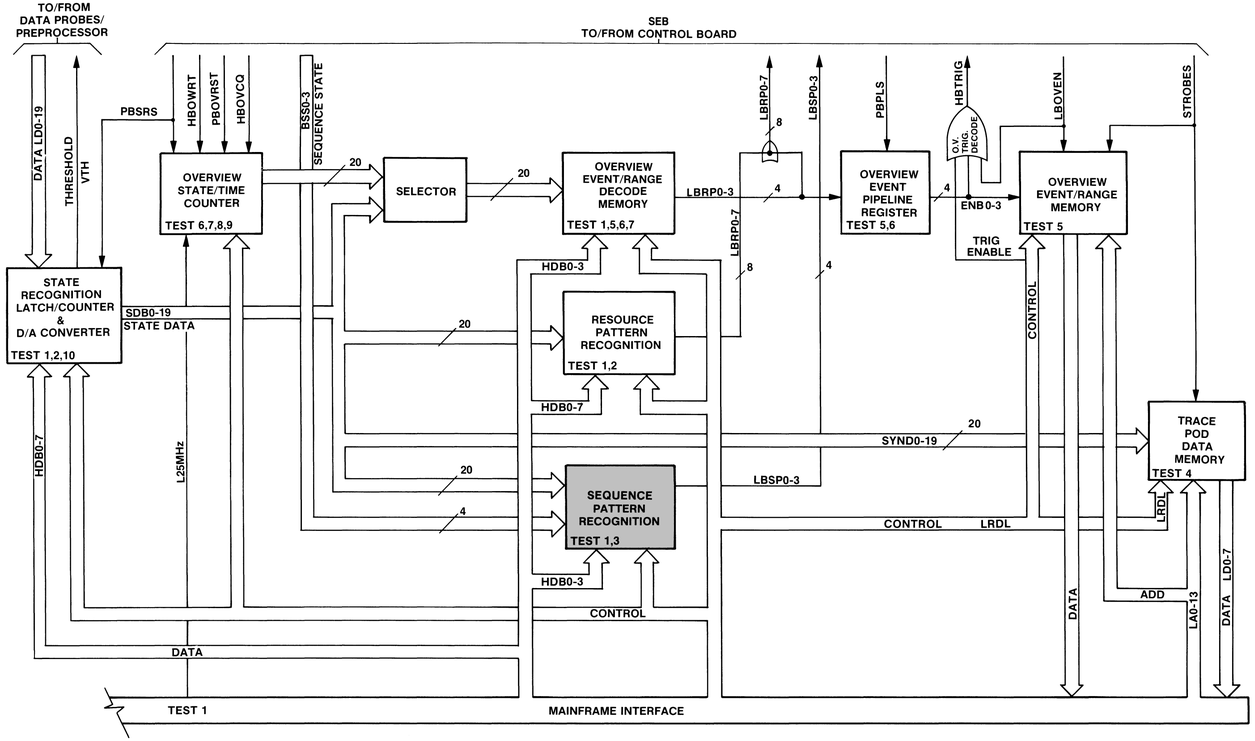
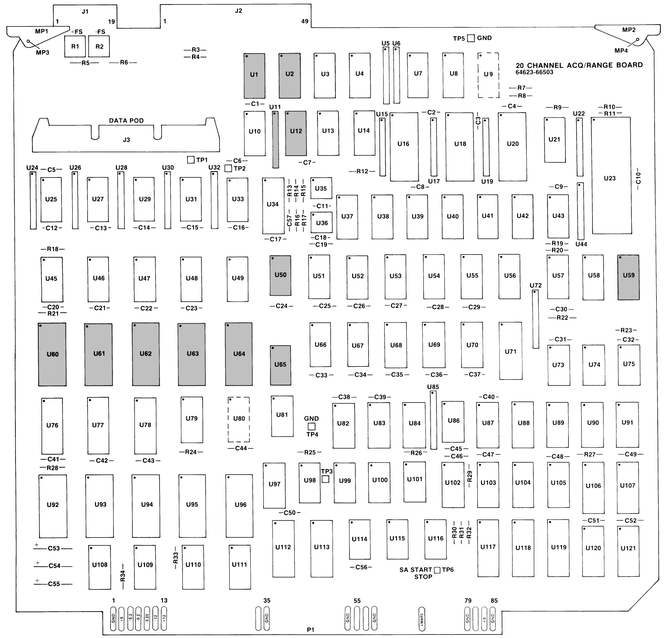


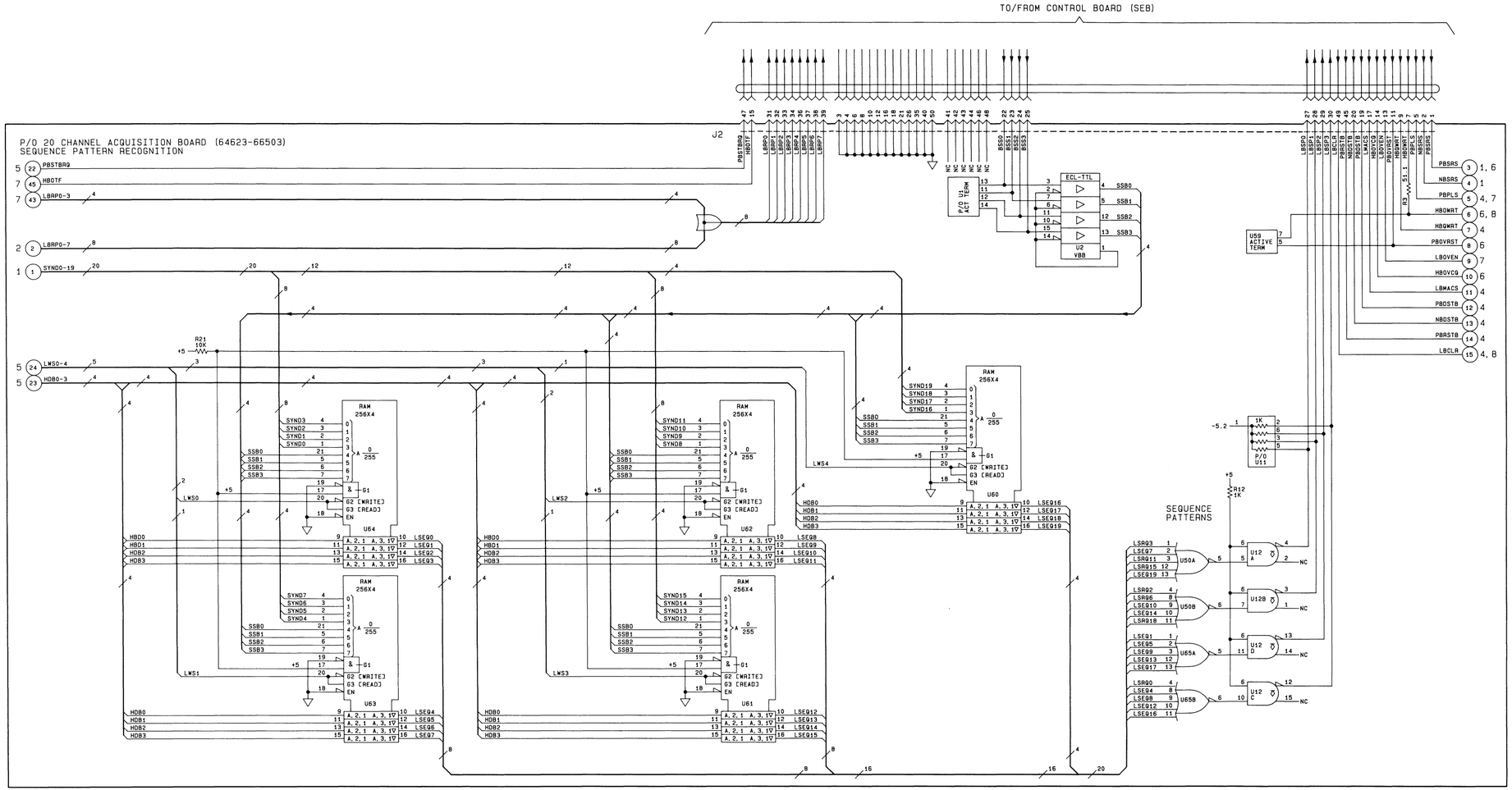
Figure 8-3.
Resource Pattern Recognition
20ACQ 8-17



Block Diagram



Component Locator



ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG PART NO.
U1	1820-2359	F10014PC
U2	1820-1052	MC10125L
U12	1820-1173	MC10124L
U50,65	1820-1275	SN74S260N
U59	1820-2359	F10014PC
U60-64	1816-1476	1816-1476

PARTS ON THIS SCHEMATIC

J2
R12,21
U1,2,11,12,50,59,60-65

IC POWER SUPPLY CONFIGURATIONS

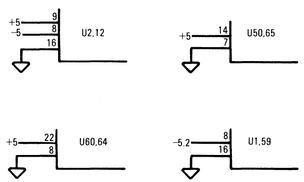
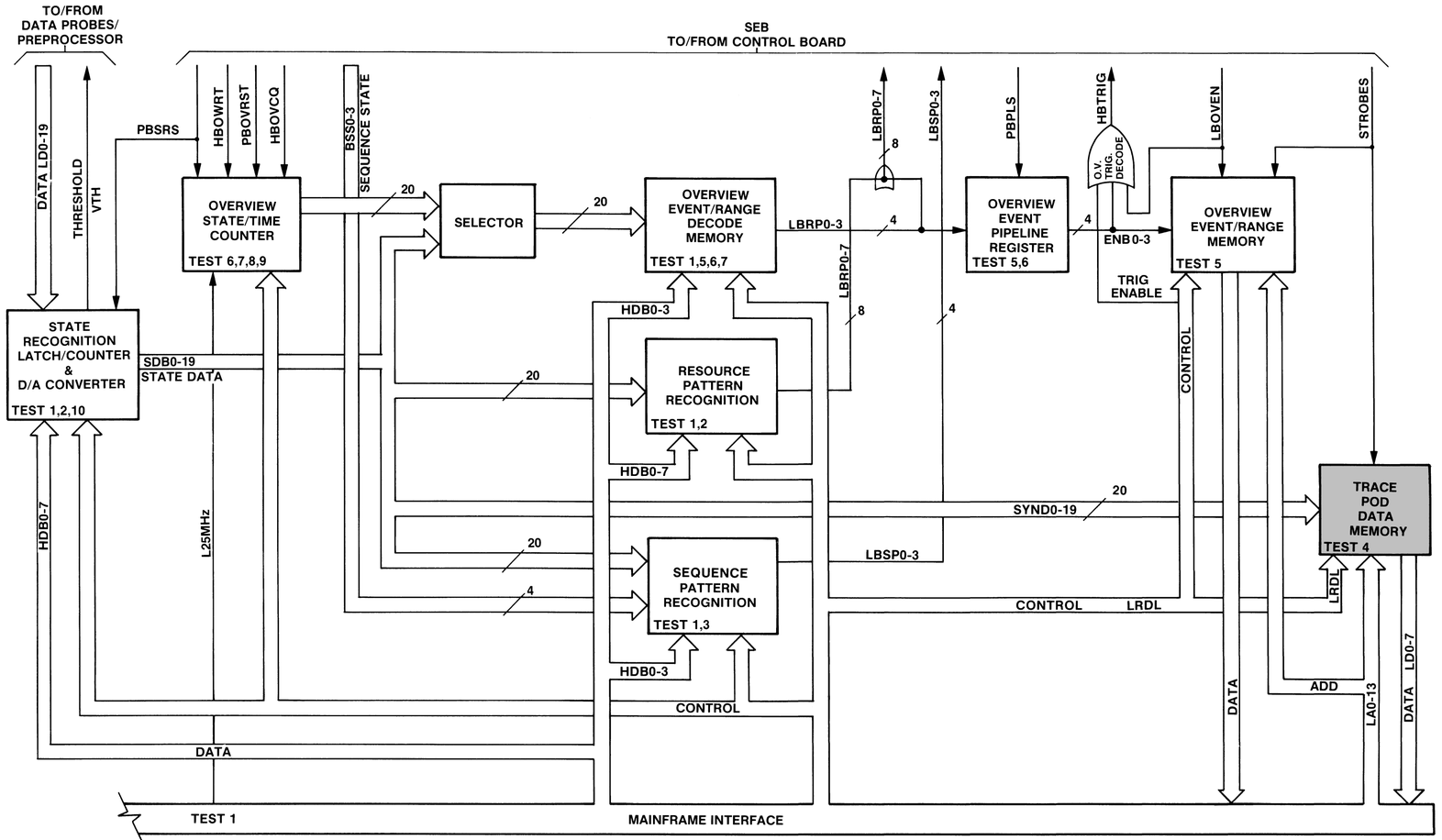


Figure 8-4.
Sequence Pattern Recognition
20ACQ 8-19



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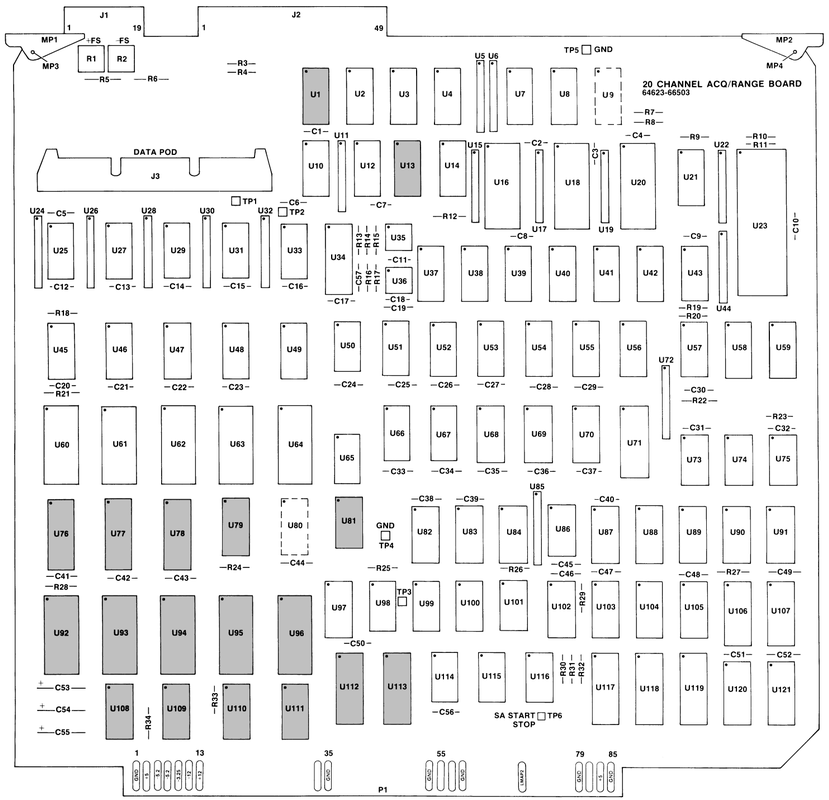
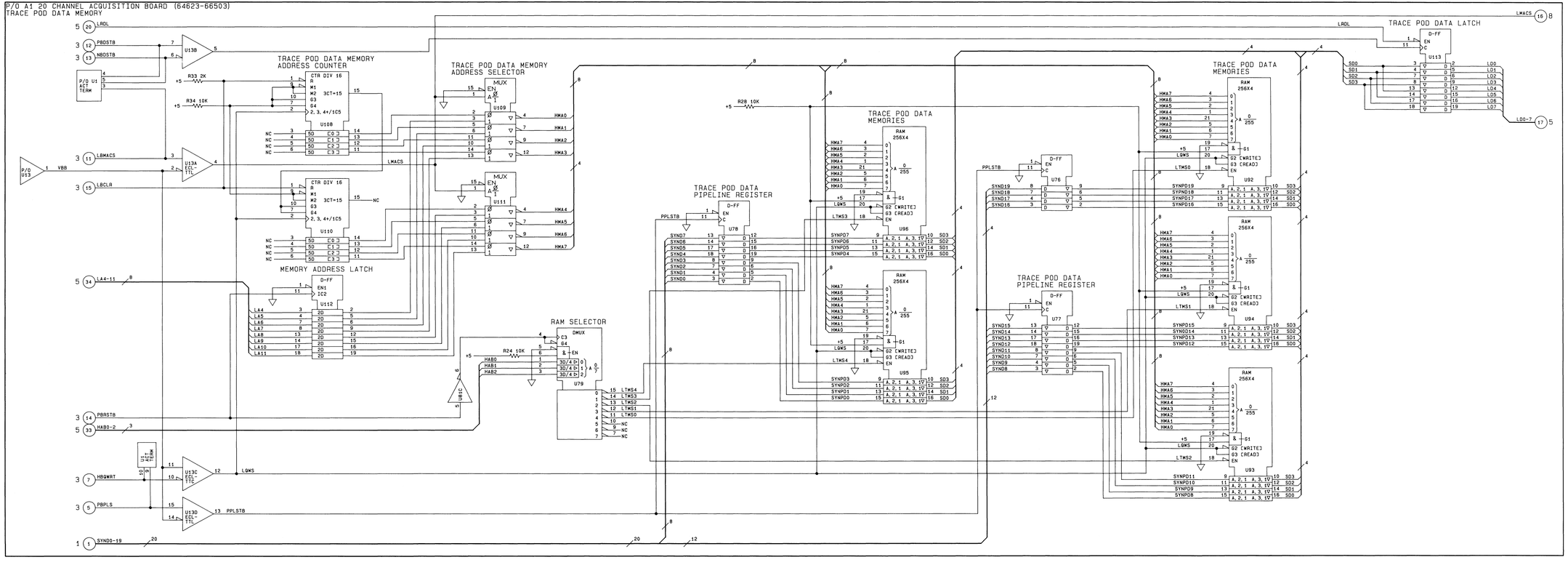


Component Locator



ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG PART NO.
U13	1820-1052	MC10125L
U76-78,113	1820-1997	SN74LS374N
U79	1820-2550	SN74LS137N
U81	1820-1199	SN74LS04N
U92-96	1816-1308	93L422PC
U108,110	1820-1430	SN74LS161AN
U109,111	1820-1428	SN74LS158N
U112	1820-1858	SN74LS377N

PARTS ON THIS SCHEMATIC

R24,28,33,34
U1,13,76-79,81,92-96,108-113

IC POWER SUPPLY CONFIGURATIONS

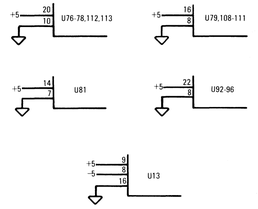
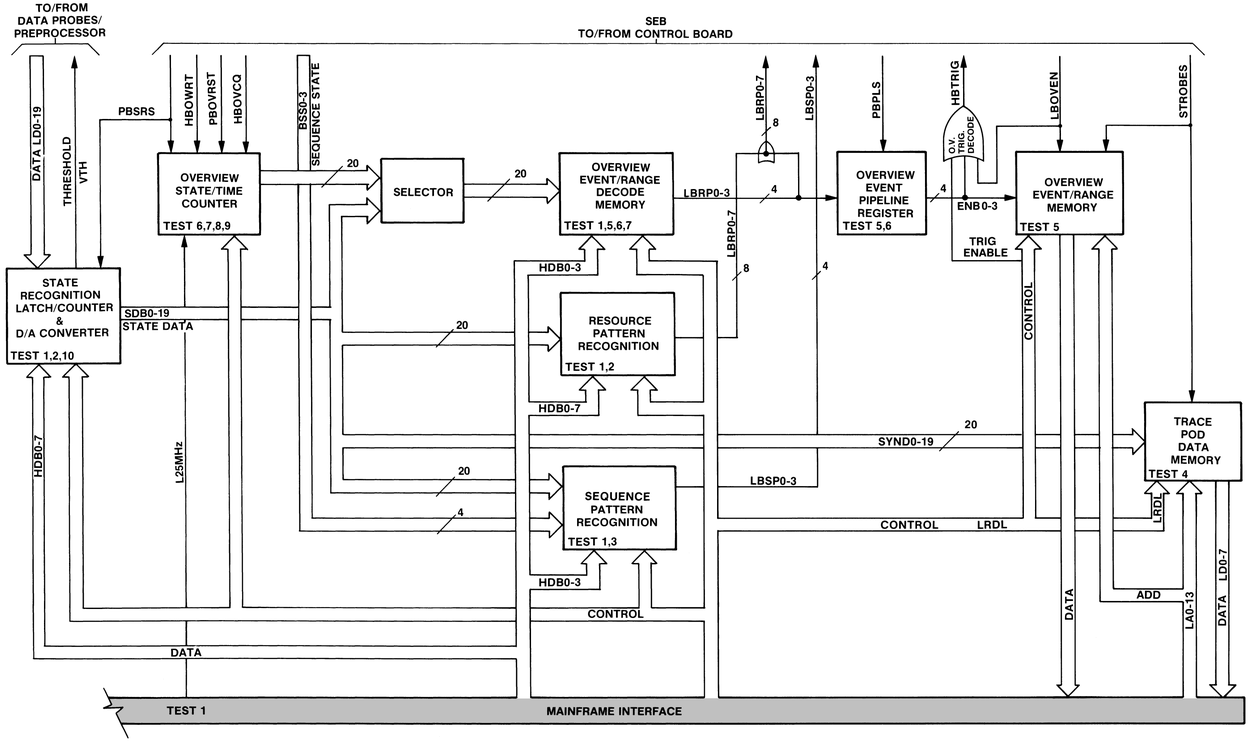
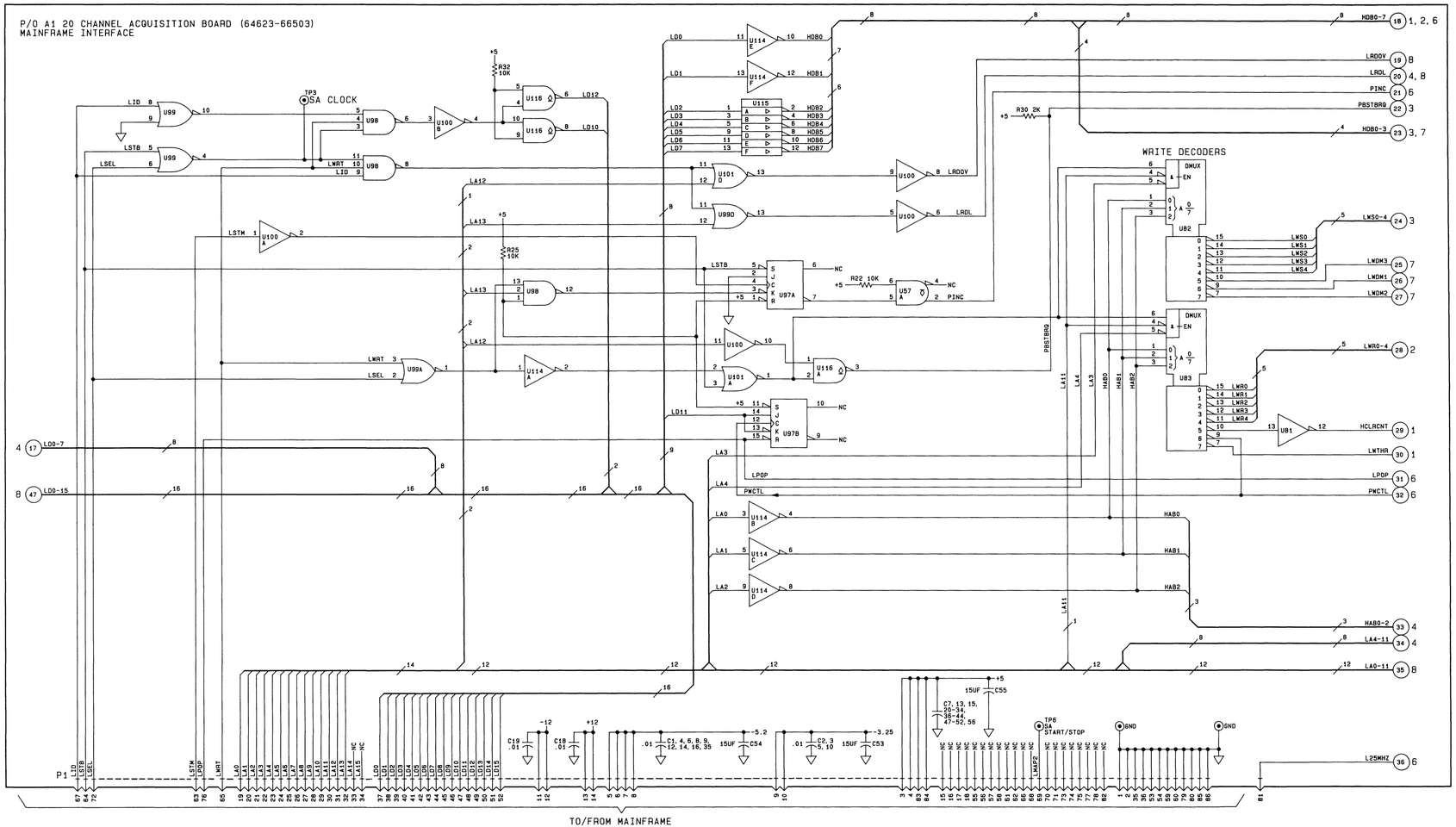


Figure 8-5.
Trace Pod Data Memory
20ACQ 8-21



Block Diagram

Component Locator



ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG PART NO.
U57	1820-1173	MC10124L
U81,100, 114,115	1820-1199	SN74LS04N
U82,83	1820-1216	SN74LS138N
U97	1820-1282	SN74LS109AN
U98	1820-1202	SN74LS10N
U99	1820-1144	SN74LS02N
U101	1820-1322	SN74S02N
U116	1820-0269	SN7403N

PARTS ON THIS SCHEMATIC

C1-10,12-16,18-44,47-56
P1
R25,30,32
TP3,4
U57,81-83,97-101,114-116

IC POWER SUPPLY CONFIGURATIONS

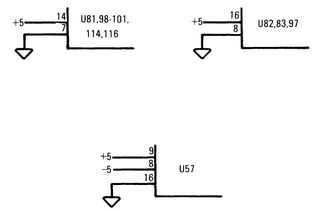
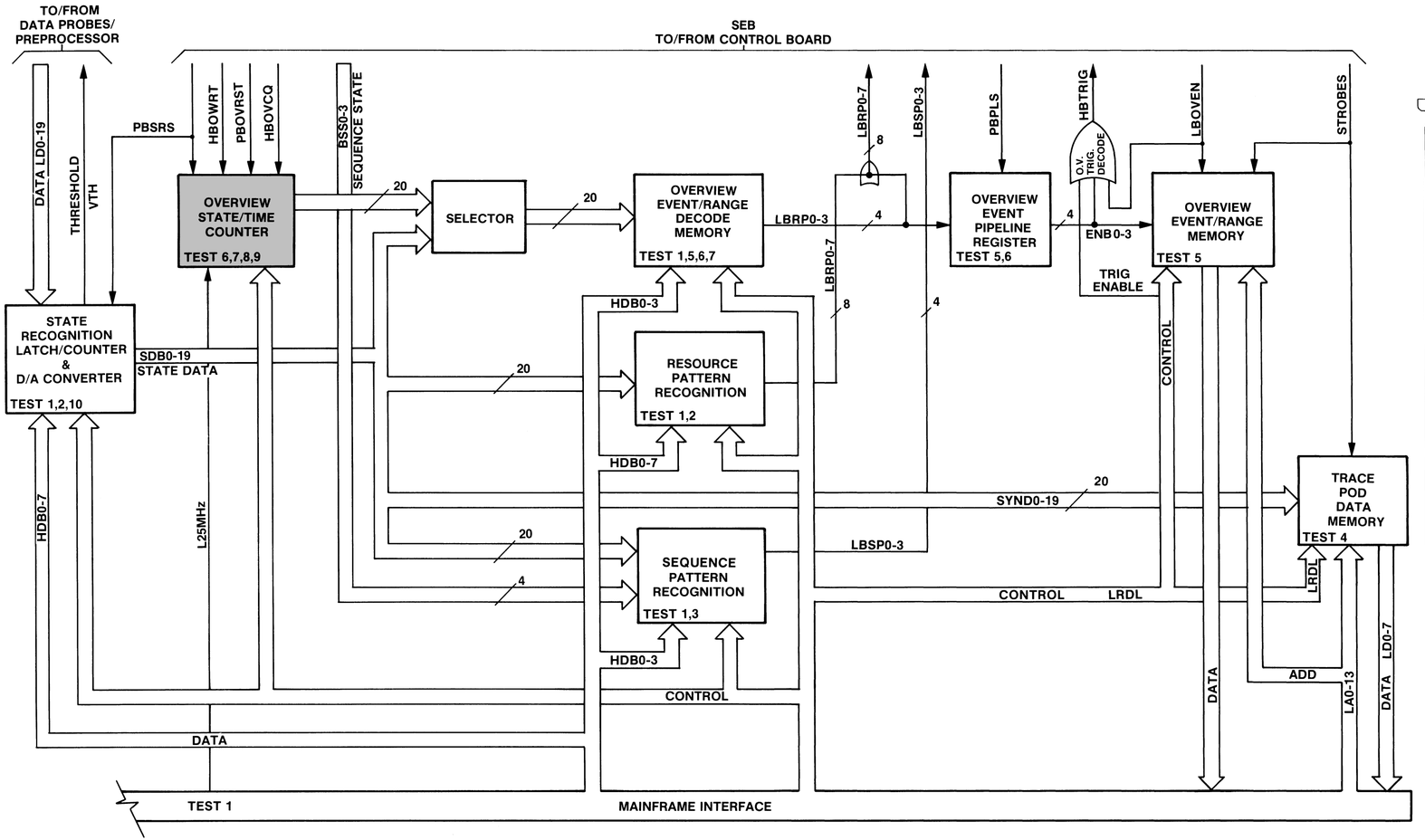
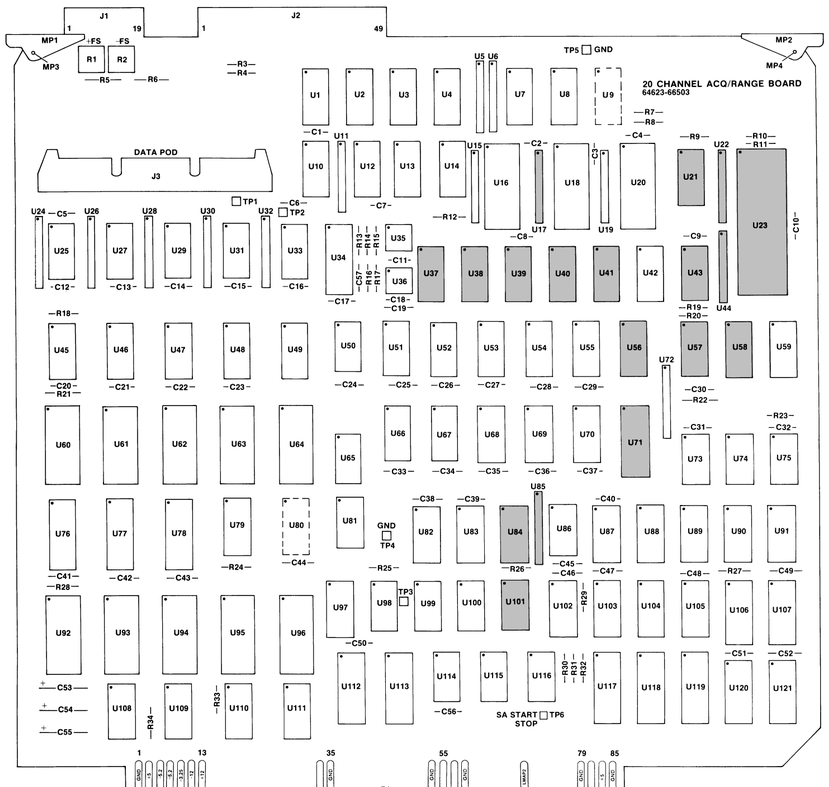


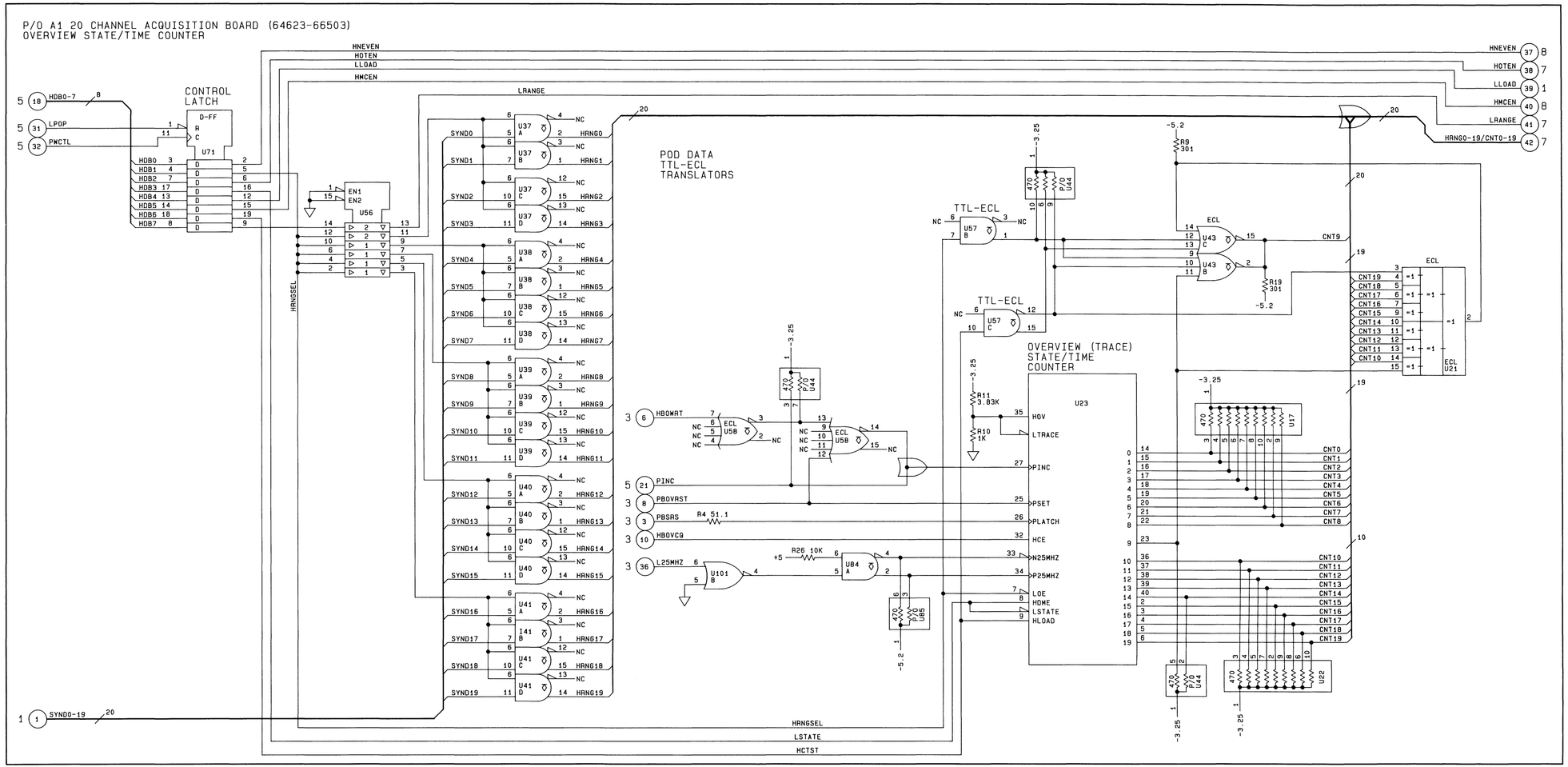
Figure 8-6. Mainframe Interface
20ACQ 8-23



Block Diagram



Component Locator



ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG PART NO.
U21	1820-0826	MC10160L
U23	INB4-5009	INB4-5009
U37-41 57,84	1820-1173	MC10124L
U43	1820-0804	MC10106P
U56	1820-1491	SN74LS367AN
U58	1820-0806	MC10109P
U71	1820-1730	SN74LS273N
U101	1820-1322	SN74S02N

PARTS ON THIS SCHEMATIC

R4,9,10,11,19,26
U17,21,22,23,37-41,43,44,56-58,71,84,85,101

IC POWER SUPPLY CONFIGURATIONS

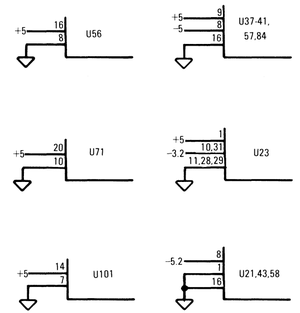
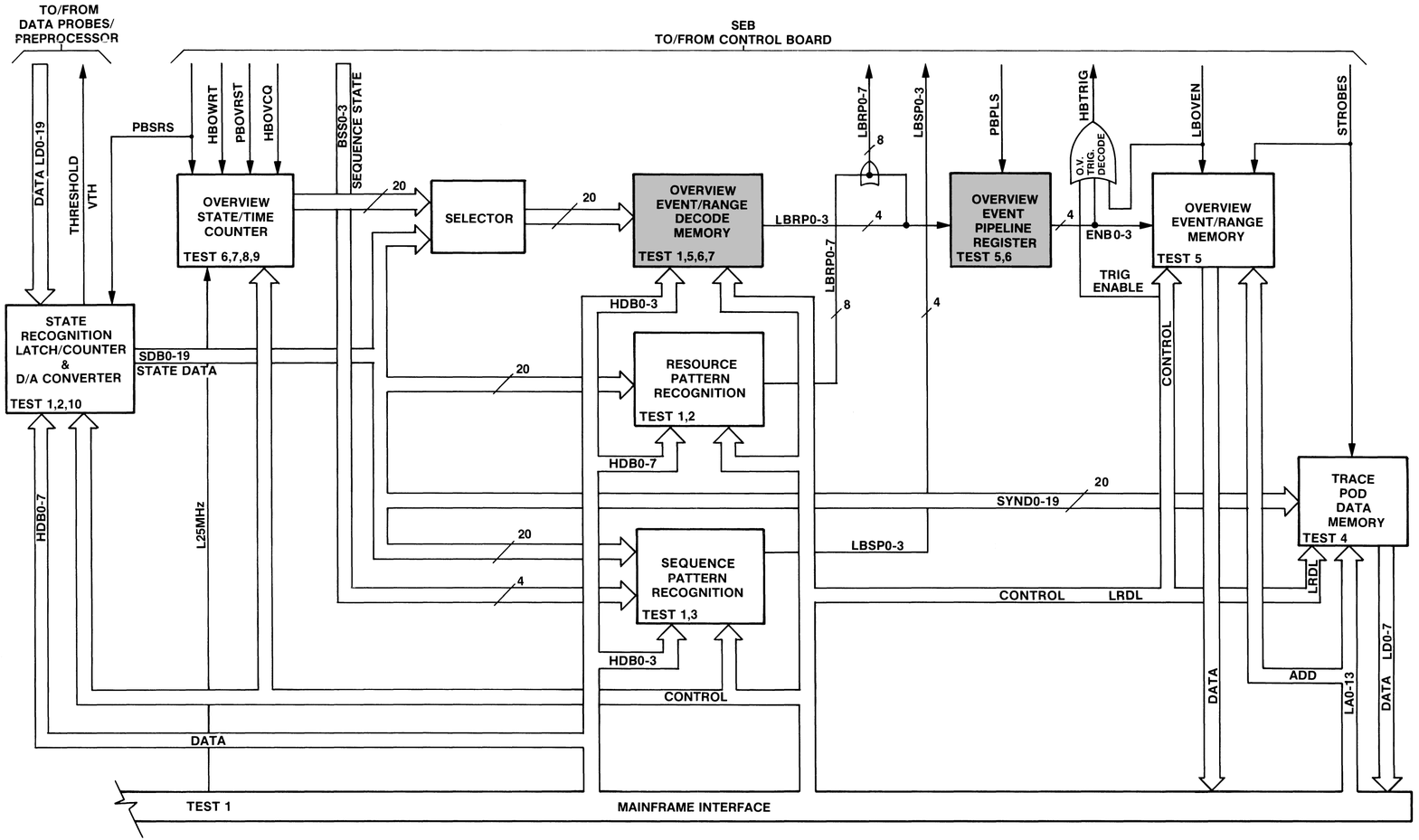


Figure 8-7. Overview State/Time Counter



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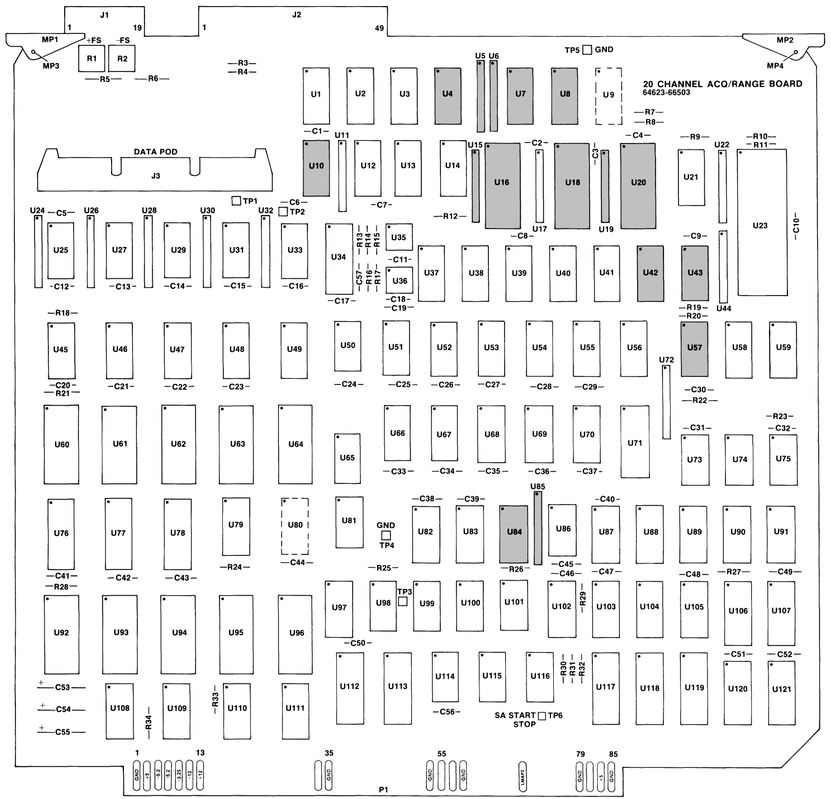
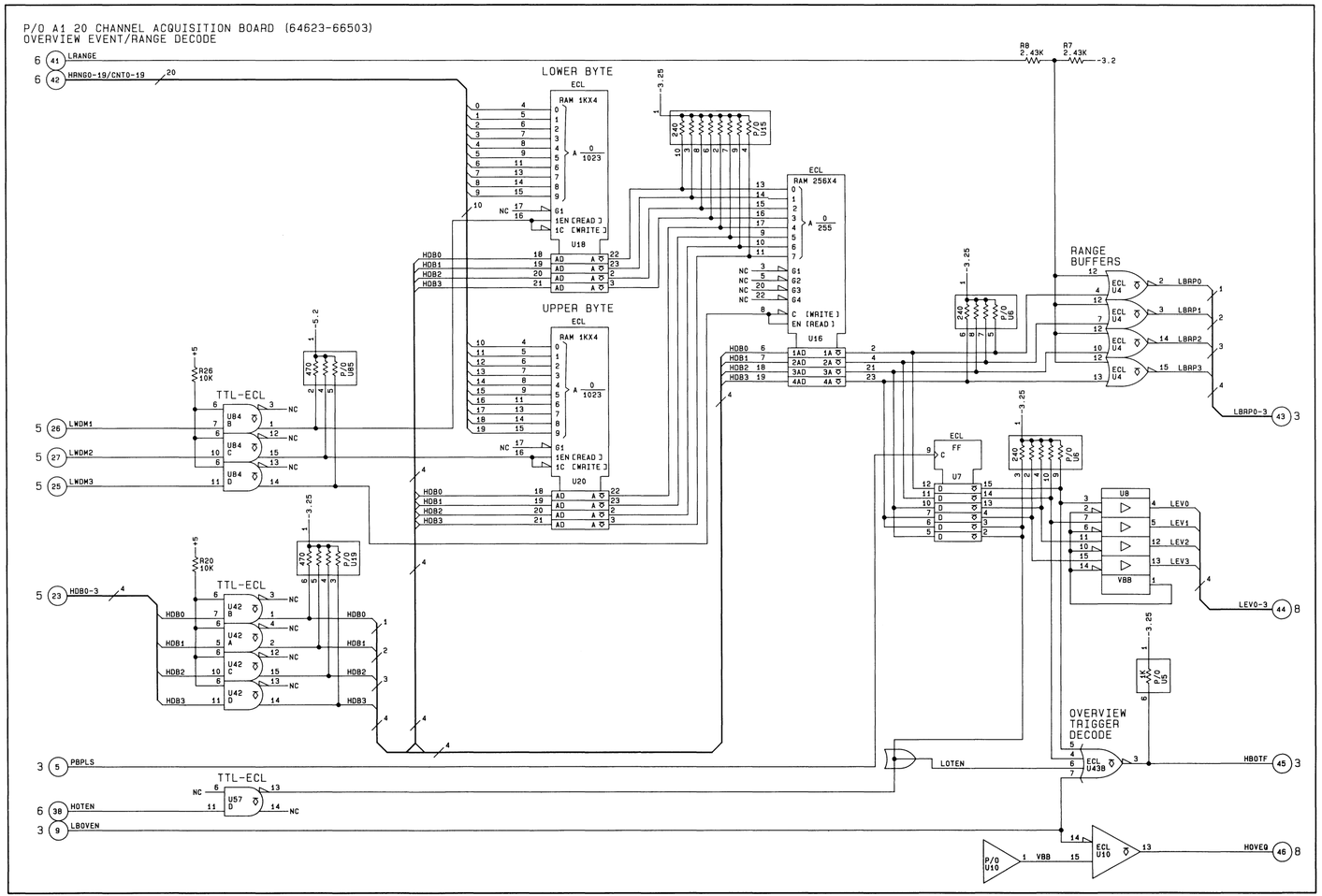


Component Locator



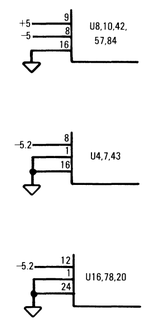
ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG PART NO.
U4	1820-0801	MC10101P
U7	1820-1399	MC10176P
U8,10	1820-1052	MC10125L
U16	1816-1462	MC10422
U18,20	1816-1492	MBM10474
U42,57,84	1820-1173	MC10124L
U43	1820-0804	MC10106P

PARTS ON THIS SCHEMATIC

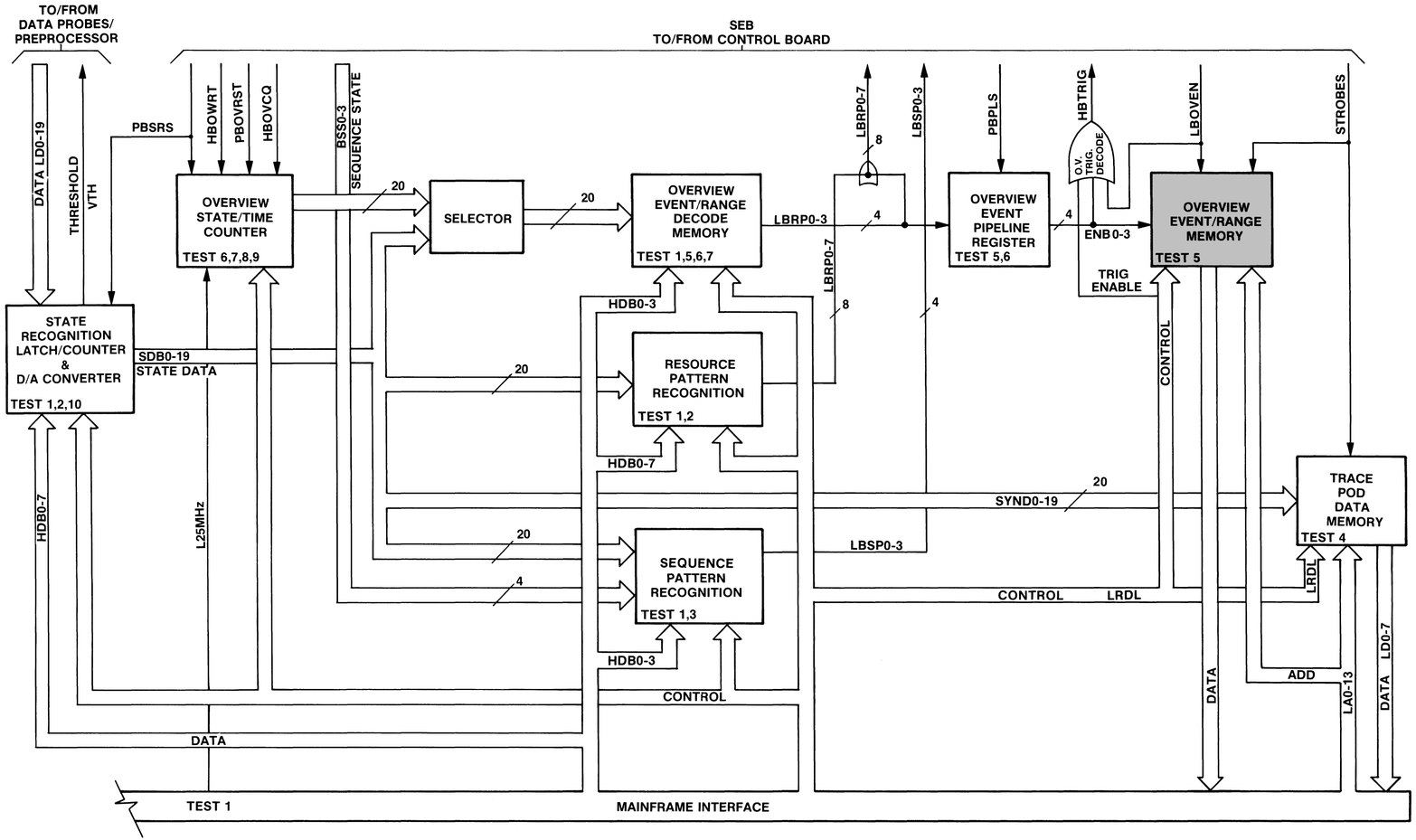
R7,8,20,26
U4-8,10,15,16,18-20,42,43,57,84,85

IC POWER SUPPLY CONFIGURATIONS

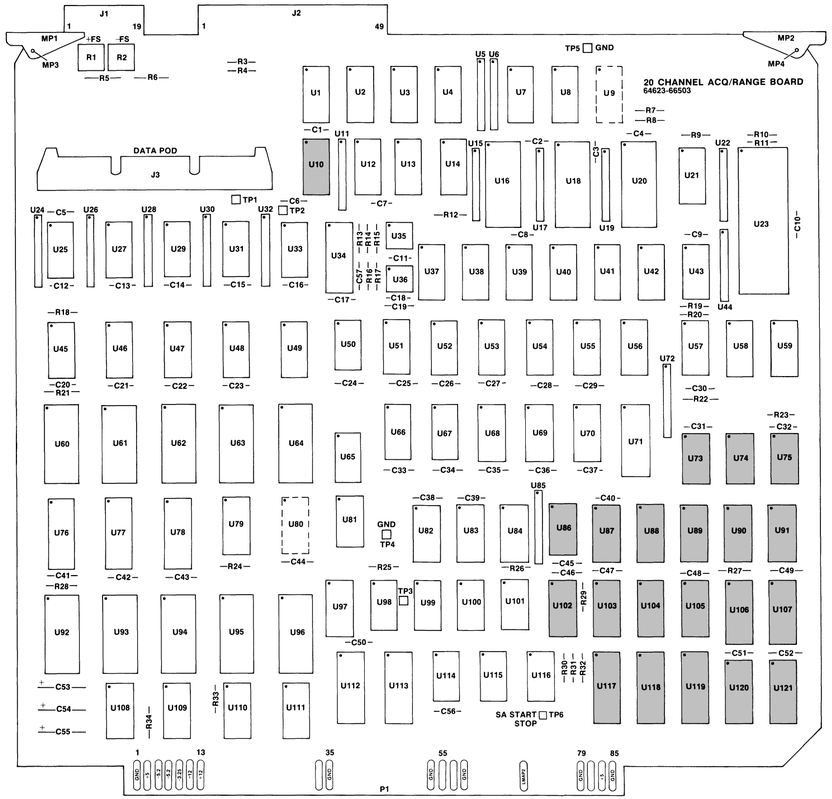


7

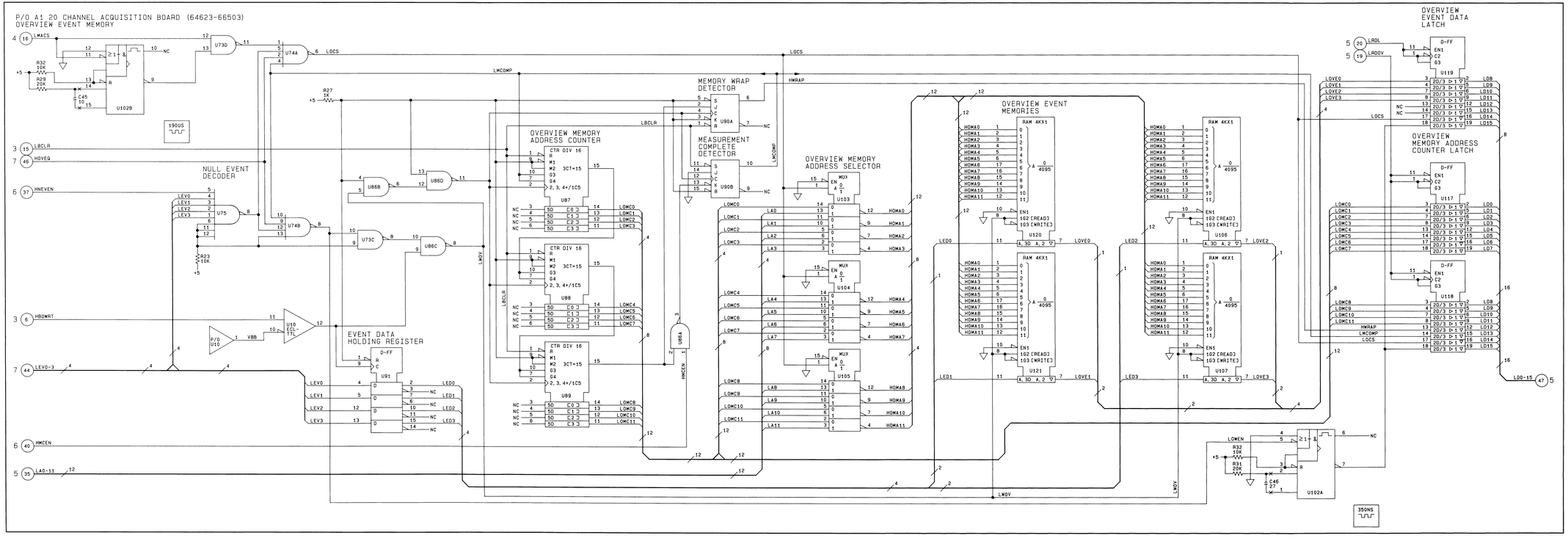
Figure 8-8.
Overview Event/Range Decode
20ACQ 8-27



Block Diagram



Component Locator



ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG PART NO.
U10	1820-1052	MC10125L
U73,86	1820-0681	SN74S00N
U74	1820-0688	SN74S20N
U75	1820-1323	SN74S30N
U87-89	1820-1430	SN74LS161AN
U90	1820-1282	SN74LS109AN
U91	1820-1191	SN74S175N
U102	1820-1782	AM26S02PC
U103-105	1820-1015	SN74S158N
U106,107	1818-1596	HM6147P-3
U117-119	1820-2102	SN74LS373
U120,121	1818-1596	HM6147P-3

PARTS ON THIS SCHEMATIC

C45,46
R23,27,29,31,32
U10,73-75,86-91,102-107,117-121

IC POWER SUPPLY CONFIGURATIONS

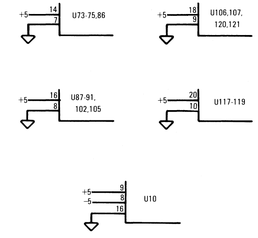


Figure 8-9.
Overview Event Memory
20ACQ 8-29

SALES & SUPPORT OFFICES
Arranged Alphabetically by Country

Product Line Sales/Support Key

Key	Product Line
A	Analytical
CM	Components
C	Computer Systems Sales only
CH	Computer Systems Hardware Sales and Services
CS	Computer Systems Software Sales and Services
E	Electronic Instruments & Measurement Systems
M	Medical Products
MP	Medical Products Primary SRO
MS	Medical Products Secondary SRO
P	Personal Computation Products
·	Sales only for specific product line
··	Support only for specific product line

IMPORTANT: These symbols designate general product line capability. They do not insure sales or support availability for all products within a line, at all locations. Contact your local sales office for information regarding locations where HP support is available for specific products.

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N-5033 **FYLLINGSDALEN** (Bergen)
Tel: (05) 16-55-40
Telex: 16621 hpnas n
CH,CS,E,MS

Hewlett-Packard Norge A/S
Österndalen 18
P.O. Box 34
N-1345 **ÖSTERÅS**
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Telex: 16621 hpnas n
A,CH,CM,CS,E,M,P

OMAN
Khimjil Ramdas
P.O. Box 19
MUSCAT
Tel: 722225, 745601
Telex: 3289 BROKER MB MUSCAT
P

Suhail & Saud Bahwan
P.O.Box 169
MUSCAT
Tel: 734 201-3
Telex: 3274 BAHWAN MB

PAKISTAN
Mushko & Company Ltd.
1-B, Street 43
Sector F-8/1
ISLAMABAD
Tel: 26875
Cable: FEMUS Rawalpindi
A,E,M

Mushko & Company Ltd.
Oosman Chambers
Abdullah Haroon Road
KARACHI 0302
Tel: 524131, 524132
Telex: 2894 MUSKO PK
Cable: COOPERATOR Karachi
*A,E,M,P**

PANAMA
Electrónico Balboa, S.A.
Calle Samuel Lewis, Ed. Alfa
Apartado 4929
PANAMA 5
Tel: 64-2700
Telex: 3483 ELECTRON PG
A,CM,E,M,P

SALES & SUPPORT OFFICES

Arranged alphabetically by country

PERU

Cía Electro Médica S.A.
Los Flamencos 145, San Isidro
Casilla 1030
LIMA 1
Tel: 41-4325, 41-3703
Telex: Pub. Booth 25306
CM,E,M,P

PHILIPPINES

The Online Advanced Systems Corporation
Rico House, Amorsolo Cor. Herrera Street
Legaspi Village, Makati
P.O. Box 1510
Metro ***MANILA***
Tel: 85-35-81, 85-34-91, 85-32-21
Telex: 3274 ONLINE
A,CH,CS,E,M

Electronic Specialists and Proponents Inc.
690-B Epifanio de los Santos Avenue
Cubao, ***QUEZON CITY***
P.O. Box 2649 Manila
Tel: 98-96-81, 98-96-82, 98-96-83
Telex: 40018, 42000 ITT GLOBE MACKAY BOOTH
P

PORTUGAL

Mundinter
Intercambio Mundial de Comércio S.A.R.L.
P.O. Box 2761
Avenida Antonio Augusto de Aguiar 138
P-LISBON
Tel: (19) 53-21-31, 53-21-37
Telex: 16691 munter p
M

Soquimica
Av. da Liberdade, 220-2
1298 ***LISBOA*** *Codex*
Tel: 56 21 81/2/3
Telex: 13316 SABASA
P

Telectra-Empresa Técnica de Equipmentos Eléctricos S.A.R.L.
Rua Rodrigo da Fonseca 103
P.O. Box 2531
P-LISBON 1
Tel: (19) 68-60-72
Telex: 12598
CH,CS,E,P

PUERTO RICO

Hewlett-Packard Puerto Rico
P.O. Box 4407
CAROLINA, Puerto Rico 00628
Calle 272 Edificio 203
Urb. Country Club
RIO PIEDRAS, Puerto Rico
Tel: (809) 762-7255
A,CH,CS

QATAR

Computearbia
P.O. Box 2750
DOHA
Tel: 883555
Telex: 4806 CHPARB
P

Eastern Technical Services
P.O.Box 4747
DOHA
Tel: 329 993
Telex: 4156 EASTEC DH

Nasser Trading & Contracting
P.O.Box 1563
DOHA
Tel: 22170, 23539
Telex: 4439 NASSER DH
M

SAUDI ARABIA

Modern Electronic Establishment
Hewlett-Packard Division
P.O. Box 281
Thuobah
AL-KHOBAR
Tel: 864-46 78
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CH,CS,E,M,P

Modern Electronic Establishment
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Telex: 202049 MEERYD SJ
CH,CS,E,M,P

SCOTLAND

See United Kingdom

SINGAPORE

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SINGAPORE 0511
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A,CH,CS,E,MS,P

Dynamar International Ltd.
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Kolam Ayer Industrial Estate
SINGAPORE 1334
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Telex: RS 26283
CM

SOUTH AFRICA

Hewlett-Packard So Africa (Pty.) Ltd.
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Howard Place **CAPE PROVINCE** 7450
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CAPE PROVINCE 7405
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Telex: 57-20006
A,CH,CM,E,MS,P

Hewlett-Packard So Africa (Pty.) Ltd.
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CH,CM

Hewlett-Packard So Africa (Pty.) Ltd.
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CH

Hewlett-Packard So Africa (Pty.) Ltd. P.O.Box 33345
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CH,E

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SPAIN

Hewlett-Packard Española S.A.
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E-BARCELONA 29
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Telex: 52603 hpbee
A,CH,CS,E,MS,P

Hewlett-Packard Española S.A.
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E-BILBAO 1
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A,CH,E,MS

Hewlett-Packard Española S.A.
Crta. de la Coruña, Km. 16, 400
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E-MADRID
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Hewlett-Packard Española S.A.
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A,CS,MS,P

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Hewlett-Packard Sverige AB
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A

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CH-1217 **MEYRIN** 1
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Hewlett-Packard (Schweiz) AG
Allmend 2
CH-8967 **WIDEN**
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SYRIA

General Electronic Inc.
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Cable: ELECTROBOR DAMASCUS
E

Middle East Electronics
Place Azmé
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DAMASCUS
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Telex: 11304 SATACO SY
M,P

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CH,CS,E

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Ing Lih Trading Co.
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Cable: INGLIH TAIPEI
A

THAILAND

Unimesa
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Telex: 84439 Simonco TH
Cable: UNIMESA Bangkok
A,CH,CS,E,M

Bangkok Business Equipment Ltd.
5/5-6 Dejo Road
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Telex: 87669-BEQUIPT TH
Cable: BUSIQUIPT Bangkok
P

TRINIDAD & TOBAGO

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PORT-OF-SPAIN
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Telex: 235,272 HUGCO WG
CM,E,M,P

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Tunisie Electronique
31 Avenue de la Liberte
TUNIS
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E,P

Corema
1 ter. Av. de Carthage
TUNIS
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Telex: 12319 CABAM TN
M

TURKEY

Teknim Company Ltd.
Iran Caddesi No. 7
Kavaklidere, ***ANKARA***
Tel: 275800
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E

E.M.A.
Medina Eldem Sokak No.41/6
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M

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Emitac Ltd.
P.O. Box 1641
SHARJAH
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Telex: 68136 Emitac Sh
CH,CS,E,M,P

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111 N. Filmore
LITTLE ROCK, AR 72205
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CH,CS

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LOS ANGELES, CA 90009
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CH,CS,E

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CH,CS

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E*,CH*,CS*

Colorado

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Brownett Building
JACKSONVILLE, FL 32207
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C*,E*,MS**

Hewlett-Packard Co.
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E*

Hewlett-Packard Co.
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ORLANDO, FL 32809
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PENSACOLA, FL 32575
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A,MS

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5750B N. Hoover Blvd., Suite 123
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Georgia

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2000 South Park Place
ATLANTA, GA 30339
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Hewlett-Packard Co.
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MS

Hewlett-Packard Co.
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SAVANNAH, GA 31401
Tel:(912) 925-5358
CH**

Hewlett-Packard Co.
P.O. Box 2103
WARNER ROBINS, GA 31099
1172 N. Davis Drive
WARNER ROBINS, GA 31093
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E

Hawaii

Hewlett-Packard Co.
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CH,MS**

Hewlett-Packard Co.
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DOWNERS GROVE, IL 60515
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Hewlett-Packard Co.
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CH,E*,MS

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A**,CH**

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160 James Drive East
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3701 Koppers St.
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Michigan

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CH,CS,MS

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MS

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A,CH,CM,E*,MS

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3
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